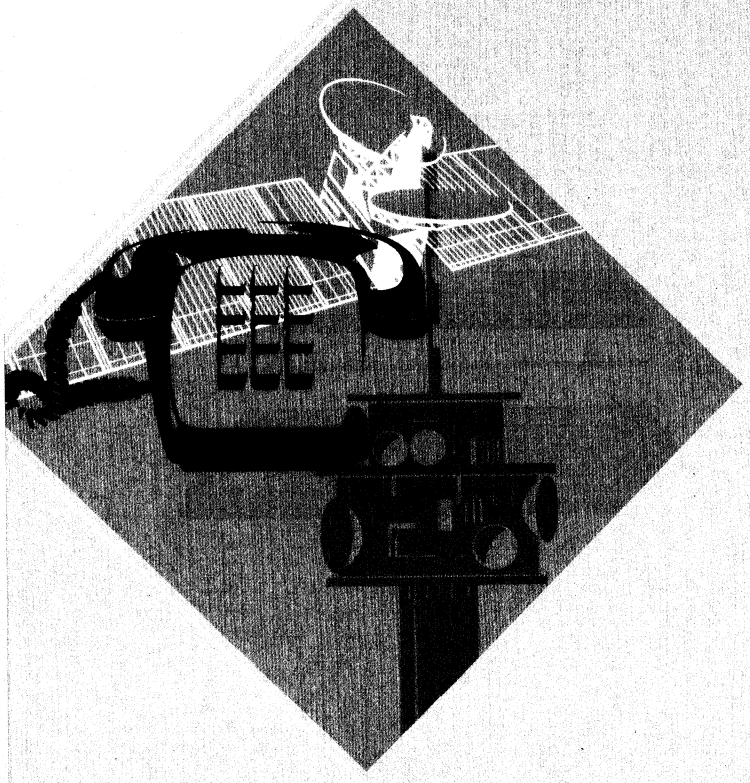

Integrated Circuits and Semiconductor Devices for Telecommunication Applications

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Contents

DF320, DF321, DF322, DF323

Loop Disconnect Dialler Circuits

Features

- Operation from 2.5 V Supply (may be unregulated)
- Low standby dissipation – 3 μW typ at 3 V supply
- Low dynamic dissipation – 540 μW typ at 3 V supply
- On-Chip oscillator uses low cost 3.579545 MHz crystal
- Power on reset
- On-Chip pull-up and pull-down terminations to inputs
- High input noise immunity: typ. 45 % of supply voltage
- Key input debounce circuitry
- Fully static storage up to 20 decimal digits
- Repeat of last number
- Selectable impulsing mark/space ratios of 2:1 or 3:2
- Selectable impulsing speeds of 10, 16, 20 and 932 Hz
- Selectable interdigital pause: 8 or 4 times impulsing period
- Hold facility to delay impulsing
- Fast data input to inhibit debounce circuitry

Applications

- Push button telephones
- Repertory diallers
- Telex
- Mobile telephone
- Security and fire alert systems
- Emergency single number call makers

Description

The DF320 series of monolithic CMOS Loop Disconnect Diallers each contain all the logic necessary to interface a standard double contact keyboard to a telephone system requiring loop disconnect signalling.

A dial pulsing output and two masking output options are provided to control the impulsing (loopdisconnect) and muting functions. The circuit is capable of storing a number string of up to 20 digits and re-dialling this stored number automatically at a later time, initiated by a RE-DIAL input code. Impulsing mark/space ratio (M/S), impulsing rate and interdigital pause (IDP) are all pin programmable to meet most telephone authority specifications.

The use of low voltage CMOS technology allows operation with an unregulated supply voltage down to a guaranteed minimum of 2.5 V. This feature, together with low operating current, negligible standby current and high noise immunity make the DF320 series easy to interface from long telephone lines.

External component count is minimised by the inclusion of an on-chip clock oscillator, high impedance pull-down terminations to programming inputs as well as pull-up terminations to the keyboard giving direct interfacing.

The four circuits DF320, DF321, DF322 and DF323 differ in the following:

The **DF320**, available in an 18-Pin Plastic Package (DF320DJ) or in an 18-Pin Side-Brazed Ceramic Case (DF320DP) provides the functions most commonly required in the pushbutton telephone application. M1 is the masking option which remains at logic '1' throughout the dialling sequence.

The **DF322**, available in Plastic Package and Ceramic Case as the DF320, is identical to the DF320 except that M2 is offered instead of M1. The M2 Masking option is at logic '1' only during impulsing, thus allowing the telephone line to be monitored during the interdigital pause.

The **DF 323**, available in Plastic Package and Ceramic Case as the DF320 and the DF322, is identical to the DF320 exept of a fixed impulsing mark/space ratio (2:1) and a selectable interdigital pause (8 or 4 times impulsing period).

The **DF321**, available in a 28-Pin Side Brazed Ceramic Case (DF321DP), is a multioption version which offers both M1 and M2 together with Fast Data Control (FD), Interdigital Pause (IDP) and System Clock internal buffer (SYS CK).

All four versions are based on the same integrated circuit.

Pin connections DF320 and DF322

1 Supply voltage V_B
2 Dial Pulse output DP
3 Output M1/M2
4 Mark/space ratio select M/S
5 Impulsing rate select F01
6 Impulsing rate select F02
7 Chip enable CE
8 Crystal input XTAL IN
9 Crystal Output XTAL OUT
10 GND, 0
11 Keyboard input X1
12 Keyboard input X2
13 Keyboard input X3
14 Keyboard input Y1
15 Keyboard input Y2
16 Keyboard input Y3
17 Keyboard input Y4
18 HOLD

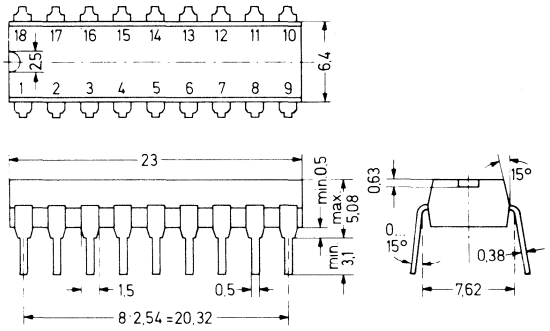


Fig. 1:
DF320DJ, DF322DJ or DF323DJ
in 18-pin Dil plastic package
20 A 18 acording to DIN 41866

Weight approximately 1.5 g
Dimensions in mm

Pin Connections DF 323

1 Supply voltage V_B
2 Dial pulse output DP
3 Output M1
4 IDP select
5 Impulsing rate select F01
6 Impulsing rate select F02
7 Chip enable CE
8 Crystal input XTAL IN
9 Crystal output XTAL OUT
10 GND, 0
11 Keyboard input X1
12 Keyboard input X2
13 Keyboard input X3
14 Keyboard input Y1
15 Keyboard input Y2
16 Keyboard input Y3
17 Keyboard input Y4
18 HOLD

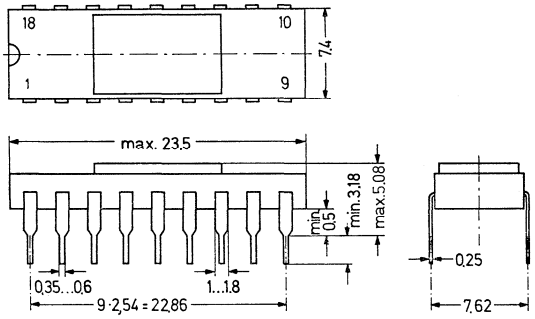


Fig. 2:
DF320DP, DF322DP or DF323DP
in 18-pin Dil side-brazed ceramic case

Weight approximately 1.7 g
Dimensions in mm

Pin Connections DF321

1 Supply Voltage V_B
2 Clock Output SYS CK
3 Dial pulse Output DP
4 N. C.
5 Output M1
6 Output M2
7 Mark/space ratio select M/S
8 IDP select
9 Impulsing rate select F01
10 Impulsing rate select F02
11 N. C.
12 Chip enable CE
13 Crystal input XTAL IN
14 Crystal output XTAL OUT
15 GND, 0
16 N. C.
17 N. C.
18 Keyboard input X1
19 Keyboard input X2
20 Keyboard input X3
21 N. C.
22 N. C.
23 Keyboard input Y1
24 Keyboard input Y2
25 Keyboard input Y3
26 Keyboard input Y4
27 Fast dial input FD
28 HOLD

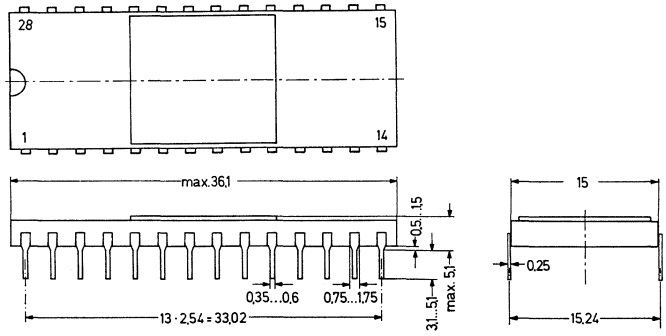


Fig. 3:
DF321 in 28-pin Dil side-brazed
ceramic case

Weight approximately 8 g
Dimensions in mm

Table 1: Pin Functions

<table>
<tr><th>Pin Function</th><th>Description (Note: O/C = Open circuit)</th></tr>
<tr><td>V_B</td><td>Positive voltage supply</td></tr>
<tr><td>SYS CK</td><td>System Clock internal buffer – for monitoring or external forcing. Frequency = 30 x Impulsing Rate. (Fig. 7)</td></tr>
<tr><td>DP</td><td>Dial Pulsing Output Buffer (Fig. 8)</td></tr>
<tr><td>M1</td><td>Mask 1 (Off Normal) Output Buffer (Fig. 8)</td></tr>
<tr><td>M2</td><td>Mask 2 Output Buffer (Fig. 8)</td></tr>
<tr><td>M/S</td><td>Mark/Space (Break/Make) Ratio select. On-chip pull-down transistor to GND. (Fig. 4)
O/C: 2:1
V_B: 3:2</td></tr>
<tr><td>IDP</td><td>Interdigital Pause. On-chip pull-down transistor to GND. (Fig. 4)
O/C: IDP = 8 x Impulsing period
V_B: IDP = 4 x Impulsing period</td></tr>
<tr><td>F01, F02</td><td>Impulsing Rate Selection. On-chip pull-down transistor to GND. (Fig. 4)
<table>
<tr><th>F01</th><th>F02</th><th>Nominal Impulsing Rate</th><th>Actual* Impulsing Rate</th><th>System Clock frequency</th></tr>
<tr><td>O/C</td><td>O/C</td><td>10 Hz</td><td>10.13 Hz</td><td>303.9 Hz</td></tr>
<tr><td>O/C</td><td>V_B</td><td>20 Hz</td><td>19.42 Hz</td><td>582.6 Hz</td></tr>
<tr><td>V_B</td><td>O/C</td><td>932 Hz</td><td>932.17 Hz</td><td>27965.1 Hz</td></tr>
<tr><td>V_B</td><td>V_B</td><td>16 Hz</td><td>15.54 Hz</td><td>466.1 Hz</td></tr>
</table>
* Assumes f_{CLK} = 3.579545 MHz.</td></tr>
<tr><td>CE</td><td>Chip Enable. An active input. Control is internal via static keyboard decode, or by external forcing. (Fig. 7)</td></tr>
<tr><td>XTAL IN</td><td>Crystal Input. Active, clamped low if CE = "0", high impedance if CE = "1" (Fig. 6)</td></tr>
<tr><td>XTAL OUT</td><td>Crystal Output. Buffer to drive crystal. Capacitive load on-chip. (Fig. 9)</td></tr>
<tr><td>GND, 0</td><td>System ground</td></tr>
<tr><td>X1, X2, X3</td><td>Column keyboard Inputs. On-chip pull-up transistors to V_B. Active LOW. (Fig. 5)</td></tr>
<tr><td>Y1, Y2, Y3, Y4</td><td>Row keyboard Inputs. On-chip pull-up transistors to V_B. Active LOW. (Fig. 5)</td></tr>
<tr><td>FD</td><td>Fast Data control. Inhibits debounce circuit to allow fast data entry from repertory dialler memory or other electronic input. On-chip pull-down transistor to GND. (Fig. 4)
O/C: Normal Operation.
V_B: Inhibit Debounce circuit.</td></tr>
<tr><td>HOLD</td><td>Prevents further impulsing. On-chip pull-down transistor to GND. (Fig. 4)
O/C: Normal Operation.
V_B: No impulsing. If activated during impulsing, hold occurs when the current digit is complete.</td></tr>
</table>

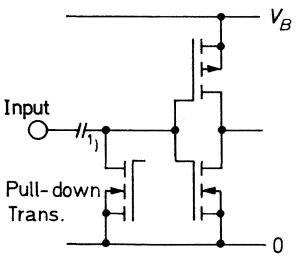


Fig. 4:
Input configuration M/S, IDP, F01, F02, FD and HOLD

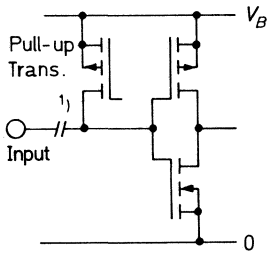


Fig. 5:
Input configuration X1 to X3 and Y1 to Y4

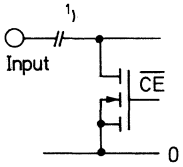


Fig. 6:
Input configuration XTAL IN

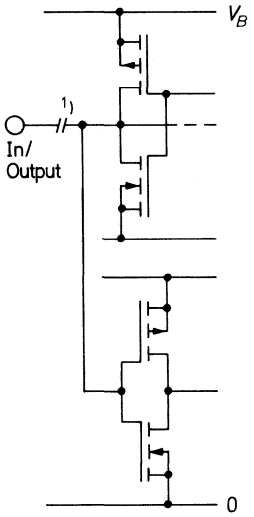


Fig. 7:
Configuration CE and SYS CK

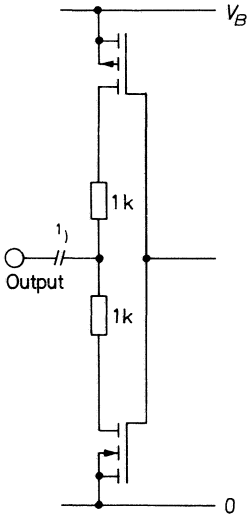


Fig. 8:
Output configuration DP, M1 and M2

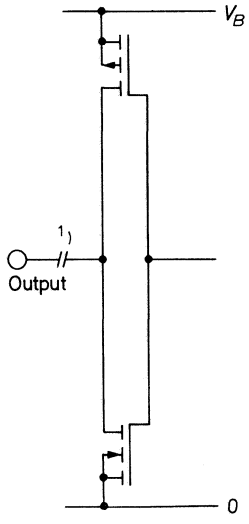


Fig. 9:
Output configuration XTAL OUT

[1]) Circuit protection not shown

All Voltages are referenced to GND unless otherwise noted

Absolute Maximum Ratings

	Min.	Max.
V_B	–0.3 V	8 V
Voltage on any pin	–0.3 V	V_B +0.3 V
Current at any pin		10 mA
Operating Temperature	–40 °C	+85 °C
Storage Temperature (P Package)	–65 °C	+150 °C
Storage Temperature (J Package)	–65 °C	+125 °C

	Min.	Max.
Power Dissipation (P Package)*	–	1000 mW
Power Dissipation (J Package)**	–	450 mW

* Derate 16 mW/ °C above 75 °C. All leads soldered to PC board.

** Derate 6.3 mW/ °C above 25 °C. All leads soldered to PC board.

Electrical characteristics

		Characteristic		Symbol	Min.	Typ*	Max.	Units	Test conditions unless noted V_B = 3.0 V, T_A = 25 °C f_{CLK} = 3.579545 MHz	
1	SUPPLY	Supply Voltage Operating Range		V_B	2.5	–	5.5	V		
2		Standby Supply Current		I_B	–	1.0	10.0	μA	CE = GND	
3		Operating Supply Current		I_B	–	180	250	μA	3.579545 MHz Crystal, $C_{XTALOUT}$ = 12 pF	
4	INPUT	Pull-Up Transistor Source Current		I_{IL}	–0.5	–3.0	–8.0	μA	V_{IN} = GND	X1, X2, X3, Y1, Y2, Y3, Y4
5		Input Leakage Current		I_{IH}	–	0.1	–	nA	V_{IN} = V_B	
6		Input Leakage Current		I_{IL}	–	–0.1	–	nA	V_{IN} = GND	M/S, IDP, F01, F02, FD, HOLD
7		Pull-Down Transistor Sink Current		I_{IH}	0.5	3.0	8.0	μA	V_{IN} = V_B	
8		Logic "0" Level		V_{IL}	–	–	0.9	V	All Inputs	
9		Logic "1" Level		V_{IH}	2.1	–	–	V		
10	OUTPUT	Voltage Levels	Low-Level	V_{OL}	–	0	0.01	V	No Load	DP, M1, M2
11			High-Level	V_{OH}	2.99	3	–	V		
12		Drive Current	N-Channel Sink	I_{OL}	0.8	2.0	–	mA	V_{OUT} = 2.3 V	
13			P-Channel Source	I_{OH}	–0.8	–1.5	–	mA	V_{OUT} = 0.7 V	
14	DYNAMIC	Output Rise Time		t_R	–	1.0	–	μs	DP, M1, M2 C_L = 50 pF	
15		Output Fall Time		t_F	–	1.0	–	μs		
16		Maximum Clock Frequency		f_{CLK}	3.58	–	–	MHz	3.579545 MHz Crystal	
17		Mark to Space Ratio		M/S	–	2:1	–		Note 1	
18					–	3:2	–			
19		Interdigital Pause		IDP	–	4T	–	ms	T = Selected impulsing Period.	
20					–	8T	–	ms	Note 1.	
21		Impulsing Rate = $\frac{1}{T}$			–	10	–		Note 1	
22					–	16	–	Hz		
23					–	20	–			
24					–	932	–			
25		Clock Start Up Time		t_{on}	–	1.5	4	ms	Timed from CE↑"1"	
26		Input Capacitance		C_{in}	–	5.0	–	pF	Any Input	

* Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.

Notes: 1. See Pin Function, Table 1.

Fig. 10:
Typical quiescent current vs. temperature

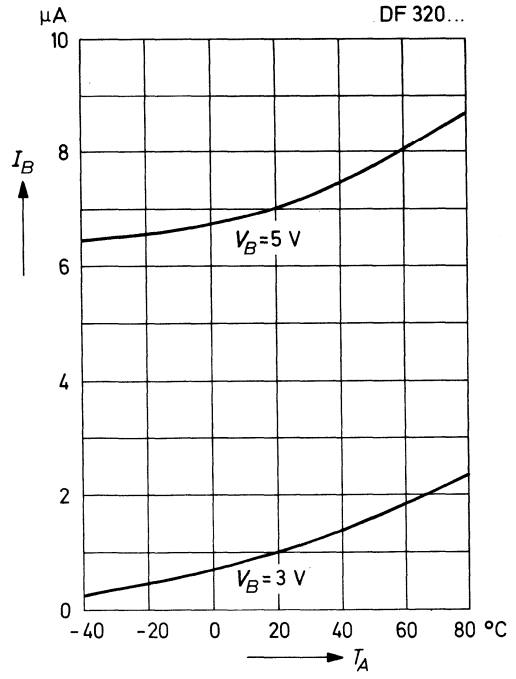


Fig. 11:
Typical dynamic current vs. supply voltage

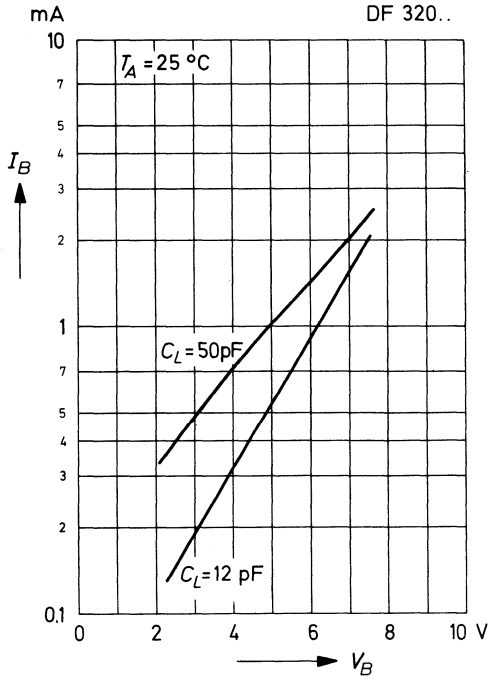


Fig. 12:
Typical percentage deviation of dynamic current vs. temperature (normalized to 25 °C)

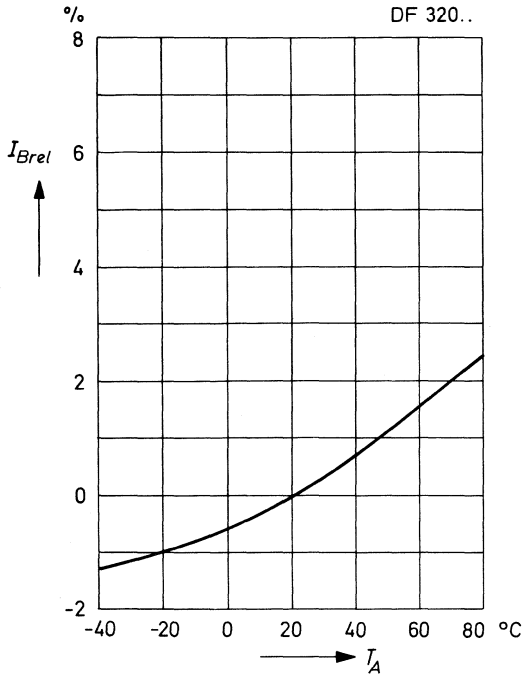


Fig. 13:
Typical XTAL IN input clamp characteristics

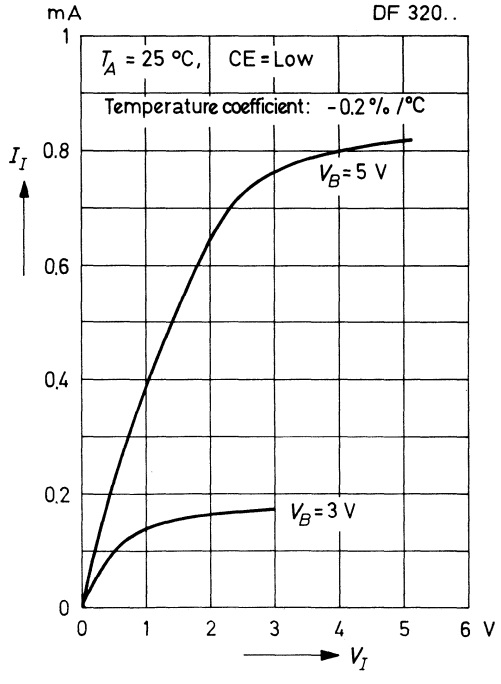


Fig. 14:
Typical input pull-up current vs. supply voltage
(X1 to X3, Y1 to Y4)

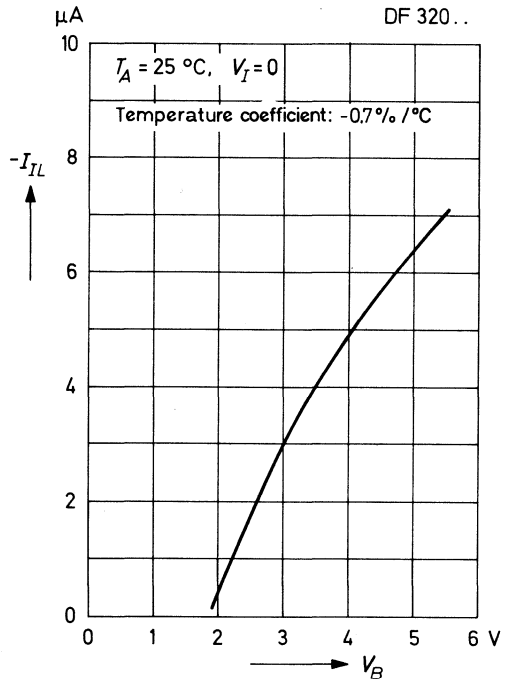


Fig. 15:
Typical input pull-up characteristics
(X1 to X3, Y1 to Y4)

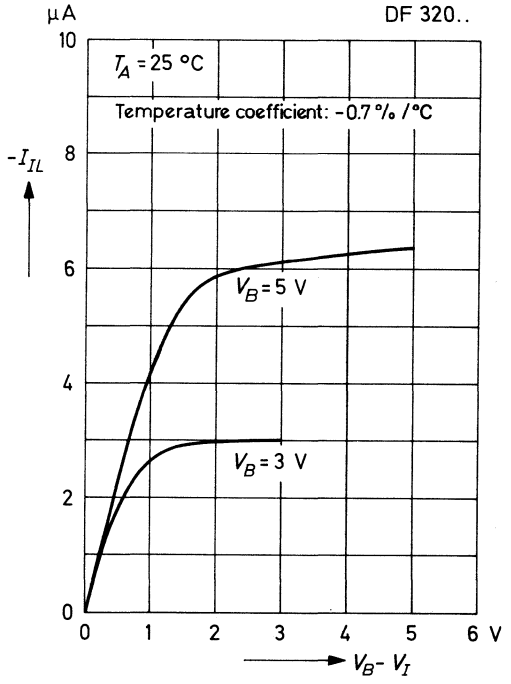


Fig. 16:
Typical input pull-down current
vs. supply voltage
(M/S, IDP, F01, F02, FD, HOLD)

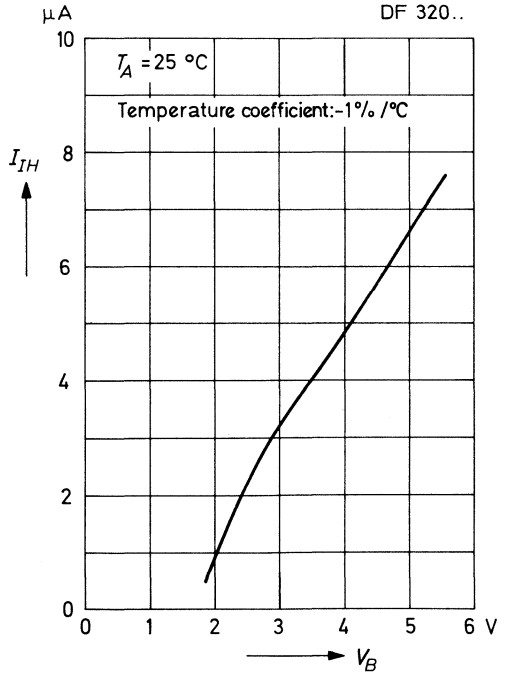


Fig. 17:
Typical input pull-down characteristics
(M/S, IDP, F01, F02, FD, HOLD)

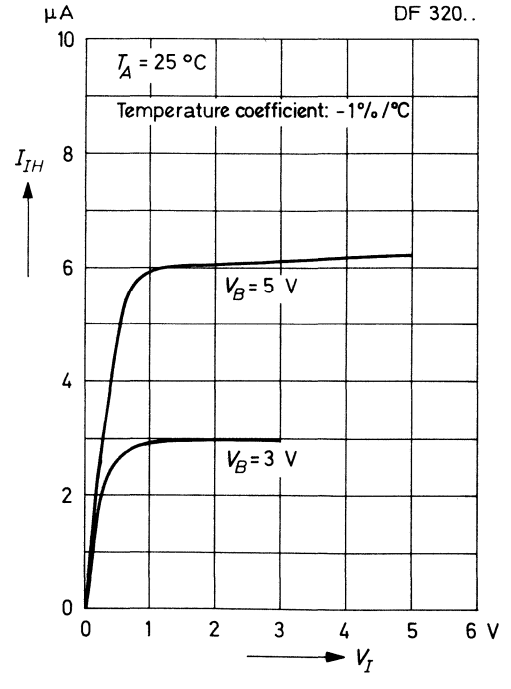


Fig. 18:
Typical chip enable sink characteristics

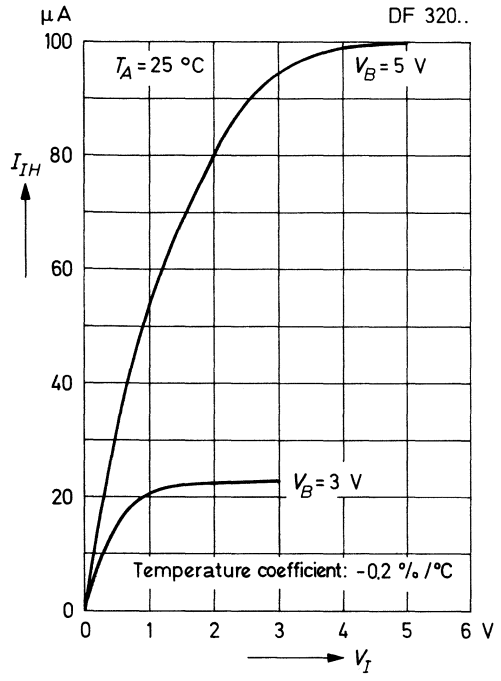


Fig. 19:
Typical chip enable source characteristics

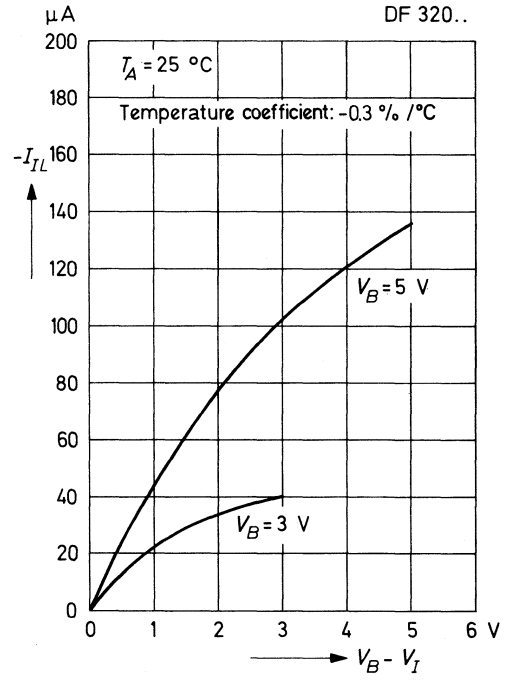


Fig. 20:
Typical output N-channel drain characteristics (DP, M1, M2)

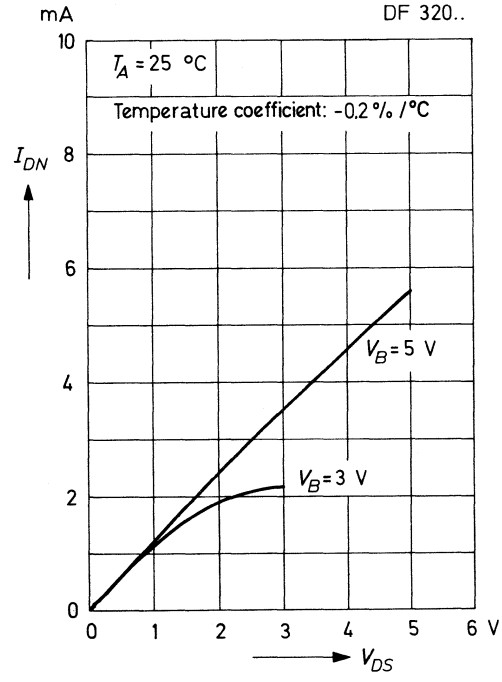
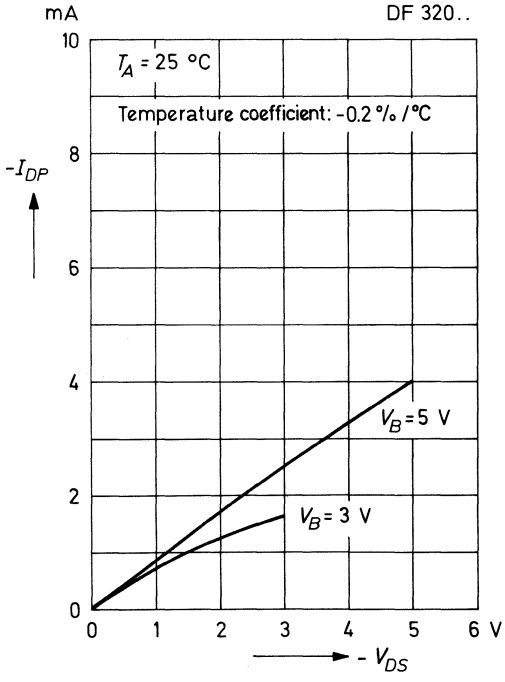


Fig. 21:
Typical output P-channel drain characteristics (DP, M1, M2)



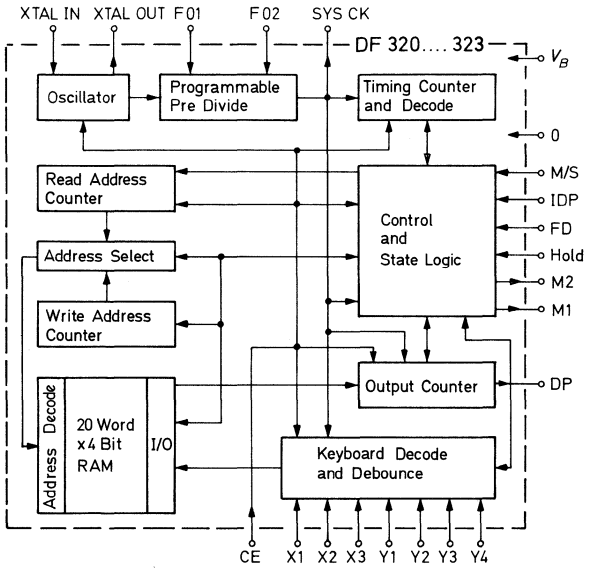


Fig. 22:
Functional block diagram

Functional Description

Clock oscillator

The on-chip oscillator amplifier is connected between the XTAL IN and XTAL OUT pins. The oscillator is completed by connecting a 3579545 Hz crystal in parallel with a 10 MΩ resistor between XTAL IN and XTAL OUT. When CE = "0" an n-channel transistor clamp is activated disabling oscillator operation. On the transition of CE to logic "1" a fast oscillator turn-on circuit kicks XTAL IN voltage to the amplifier bias point allowing oscillator operation within 4 msec. The basic clock frequency of 3.58 MHz is predivided by a programmable counter to provide the chip system clock. This is available on pin 2 of the DF321 and is usable to synchronize external logic if required.

As an alternative an LC oscillator can be formed as shown in Fig. 31. Selection of f_{CLK} = 38.4 kHz with F01 connected to V_B will give an impulsing rate of 10 Hz. It is also possible to control the DF320, DF321, DF322, DF323 from an external clock applied to XTAL IN.

Chip enable, CE

The Chip Enable pin is used to initialise the chip system. CE = "0" conditions the chip to the static standby mode. In this mode the clock oscillator is off, internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER and the circuit is ready to receive a new number or re-dial. Whilst CE = "0" data cannot be received by the chip, but data previously entered and stored is maintained. When CE = "1" the clock oscillator is operating, the internal registers are enabled, and data can be entered from the keyboard up to a maximum of 20 digits.

CE is primarily controlled by a logic gate with function

F = KEYBOARD INPUT + M1 + HOLD

where + denotes logical OR.

To operate this gate, a resistor and capacitor should be connected in parallel between CE and GND. When the chip is used in the CE INTERNAL CONTROL MODE power on reset occurs when V_B is applied, since a logic "0" appears on the CE pin. The chip remains in the static standby condition until it receives the first valid keyboard input after V_B is applied. This is statically decoded and causes CE = "1", hence enabling the clock oscillator. The debounce counter is then clocked by the system clock until the valid data condition is recognised. Data is then written into the on-chip RAM. CE is maintained at logic "1" by M1 during dialling.

The WRITE ADDRESS COUNTER is reset on recognition of the first valid debounced keyboard input provided that it is decoded during t_d of the pre-impulsing pause PIP (see Fig. 23). In the CE INTERNAL CONTROL MODE this condition will always apply. When all keyed digits have been dialled, M1 goes to logic "0" and hence the chip returns to the static standby condition. If digits are subsequently keyed during the same off-hook period, after a pause in dialling for example, the digit string will be recognised as a new number. This is not important provided RE-DIAL operation is not required.

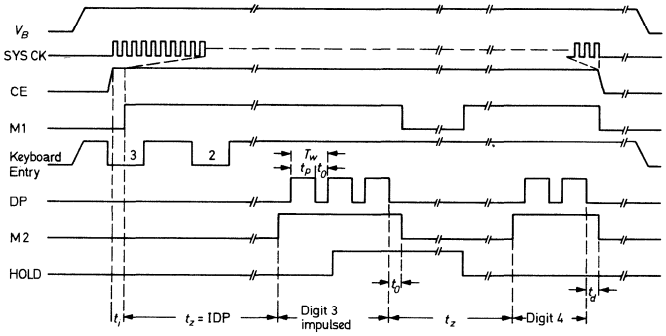


Fig. 23:
Loop disconnect dialler timing diagram, CE internal control
Note: $t_i = t_{on} + t_d$ where t_{on} = Clock Start Up Time

The alternative to the CE INTERNAL CONTROL MODE is to override the internal logic gate with an externally derived signal. This mode of operation is referred to as the CE EXTERNAL CONTROL MODE. Reference to Fig. 24 shows that if CE goes to logic "1" in the absence of a keyboard input, a single pulse of duration t_d is generated on M1. This pulse is intended to initialise a bistable latching relay used as shown in Fig. 28. Immediately prior to M1 going to logic "1" the WRITE ADDRESS COUNTER is reset. All digits keyed subsequently are entered into consecutive RAM locations up to a maximum of 20. After the WRITE ADDRESS COUNTER has been reset, the RE-DIAL input code will not be recognised by the circuit. It is necessary that CE be maintained at logic "0" > 1 μsec after V_{DD} is applied in order to ensure correct system initialising. If CE is linked to V_B by the method shown in Fig. 28, adequate delay is obtained.

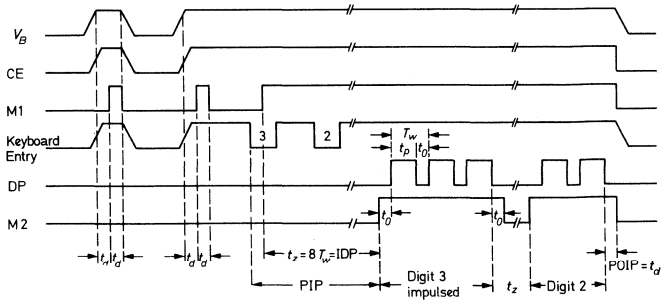


Fig. 24:
Loop disconnect dialler timing diagram. CE external control

Notes:
1. $t_d = 10 \times P$
   P = System clock period = $\frac{T}{30}$
   T is selected impulsing period
2. Pre-Impulsing Pause (PIP) = [(8T or 4T) + t_d]
3. Post-Impulsing Pause (POIP) is equal to t_d ms
4. t_b/t_m is the BREAK/MAKE RATIO. T = (t_m + t_b) ms.
   t_m = 10 x P for 2:1 M/S ratio. t_m = 12 x P for 3:2 M/S ratio.

Data Entry

Data is entered to the circuit via a double contact keyboard connected as shown in Fig. 26. Keyboard inputs are active low and encoded as shown in Table 2.

Table 2: Keyboard code

No. of O/P Pulses	Digit	Y1	Y2	Y3	Y4	X1	X2	X3
1	1	0	1	1	1	0	1	1
2	2	0	1	1	1	1	0	1
3	3	0	1	1	1	1	1	0
4	4	1	0	1	1	0	1	1
5	5	1	0	1	1	1	0	1
6	6	1	0	1	1	1	1	0
7	7	1	1	0	1	0	1	1
8	8	1	1	0	1	1	0	1
9	9	1	1	0	1	1	1	0
10	0	1	1	1	0	1	0	1
RE-DIAL		1	1	1	0	1	1	0

Note: "0" indicates pin taken low.

Keyboard inputs are fully decoded eliminating any possibility of invalid codes being recognised. A BCD format is used on-chip for data storage. Valid inputs have contact bounce removed via the debounce counter. Operation is illustrated in Fig. 25. Input data is not written into the RAM until the input code has been present for a minimum of 3P and maximum of 4P (P = System Clock Period). The 1P uncertainty arises since data entry is not synchronized to the system clock. This is indicated by the shaded area on the keyboard entry waveform of Fig. 25. The trailing edge of a keyboard entry is also debounced. The operation of the debounce circuitry results in a maximum data entry rate of SYS CLK ÷ 9. Referring to Fig. 25, data must remain stable during the RAM data entry period. Maximum contact bounce rejection is 10 msec at 10 Hz, 6.3 msec at 16 Hz or 5 msec at 20 Hz impulsing rates. Minimum data valid time is 16.7 msec at 10 Hz, 10.4 msec at 16 Hz or 8.4 msec at 20 Hz impulsing rates.

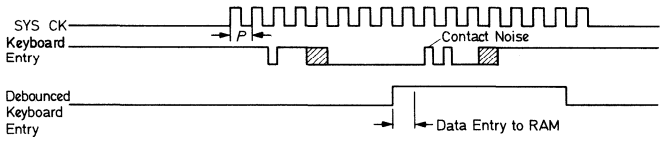


Fig. 25:
Keyboard input debounce timing diagram

On the DF321, FD is provided to inhibit the debounce circuitry and allow "fast data" entry. When FD = "1" valid keyboard codes may be entered at a maximum rate defined by a data valid time of 2P and an interval between data entry of 1P. This is equivalent to 200 Hz at the 20 Hz impulsing rate. Data need not be synchronized to the system clock since synchronization is provided on-chip.

Upon recognition of the first keyboard input of a number string the dial out sequence is initiated by a pre-impulsing pause (Fig. 24). The WRITE ADDRESS COUNTER is incremented on each digit entry. The contents of this counter indicate the length of the number to be dialled and reset is not caused by CE = "0". The RE-DIAL code is recognised only if it is presented to the chip a maximum of 5P after CE = "1". Decoding of RE-DIAL then inhibits the reset of the WRITE ADDRESS COUNTER, initiates the dialling sequence and the previous number string entered is dialled. If the circuit application is to utilize RE-DIAL, external CE control is necessary in some cases to ensure that CE = "1" from the first keyboard entry throughout dialling in order to ensure all digits entered are stored consecutively should a delay occur during number keying.

Dialling sequence

The dialling or impulsing sequence is initiated on recognition of the first keyboard entry after CE = "1". The dialling sequence is identical for both internal and external control of CE. See Figs. 23 and 24.

The basic impulsing pulse train is derived from the TIMING COUNTER AND DECODE. The IDP is timed by forcing a code on the OUTPUT COUNTER and inhibiting DP for the duration of IDP. The READ ADDRESS COUNTER then addresses the RAM and the first digit is used to program the decode of the OUTPUT COUNTER. A number of dial pulses is output via DP corresponding to the BCD data read from the RAM. At the completion of the digit, the READ ADDRESS COUNTER is incremented. The sequence continues until coincidence is recognised between the READ ADDRESS COUNTER contents and the WRITE ADDRESS COUNTER contents. The post-impulsing pause, POIP, is then output. The circuit then enters the dynamic standby condition if CE is maintained at logic "1" by external control, or the static standby condition if CE INTERNAL CONTROL MODE is used.

Impulsing rates, impulsing mark-to-space ratio and interdigital pause are programmable as shown in Table 1.

The dialling sequence can be interrupted by applying logic "1" to HOLD. If HOLD = "1" is applied during dialling of a digit, the circuit does not enter the HOLD mode until the digit is complete. In the HOLD mode M1 = "0" allowing the telephone line to be monitored. When HOLD is released dialling continues preceded by an IDP (see Fig. 23). HOLD is used to extend the IDP allowing intermediate dial tone recognition if RE-DIAL is used in a PABX for example. Operation can be manual or via external control logic as shown in Fig. 29.

Notes:

(i) The keyboard input decoding is mask programmable to suit different input codes.
(ii) The timing circuitry is mask programmable to give different M/S ratios.
(iii) The clock predivision circuitry is mask programmable allowing use of different crystal or external clock frequencies.
(iv) The logic sense of DP, M1 and M2 outputs is mask programmable.

Applications

The circuit of Fig. 26 shows a method of connecting the DF320 in parallel with the telephone network.

When the handset is lifted and power applied to the circuit T_2 is fed base current through R_2 which in turn drives T_1. C_2 is charged via R_3 in series with D_1 to $(V_{Z1} - 0.7)$ V. When the minimum operating V_B voltage is reached, power on reset occurs via the CE network of C_1 and R_8. T_2 is maintained in the "ON" condition by G_1 whilst T_3 and hence T_4 are held off by G_2. The DF320 network appears in parallel with the telephone as an impedance > 10 kΩ in the standby condition with the telephone network connected in circuit through T_1.

On recognition of the first keyed digit the DF320 clock is started. M1 then goes to logic "1" causing T_2, T_1 to turn off, and T_3, T_4 to turn on. Hence the majority of the line loop current now flows

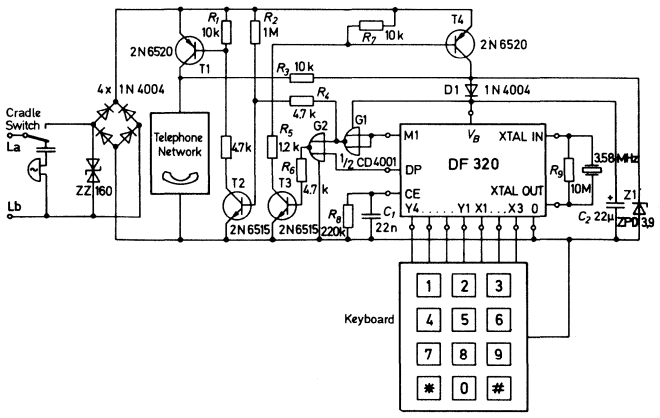


Fig. 26:
DF320 Parallel Telephone Connection

through T_4, and Z_1. When impulsing occurs T_3 and T_4 are turned off by DP acting on G_2. Line loop current is then reduced to approximately 50 µA taken through R_2, R_4 and G_2 in series.

When dialling is complete M1 goes to logic "0" causing the telephone network to be reconnected. The DF320 then returns to the static standby condition. If the line loop is interrupted by the cradle switch during dialling, impulsing will continue until C_2 discharges to a voltage such that R_8 pulls CE to logic "0" causing the DF320 to reset.

The diode bridge protects the network from line polarity reversal.

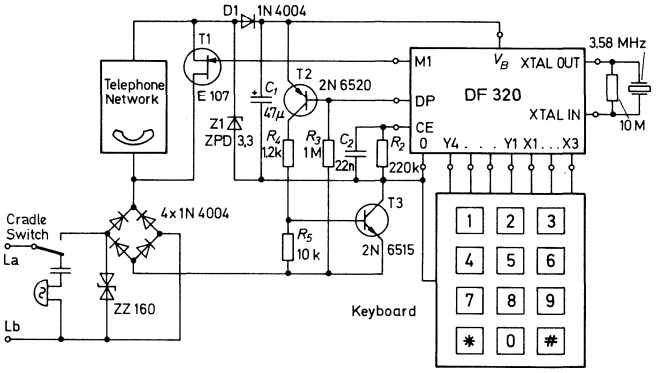


Fig. 27:
DF320 Series Telephone Connection

The circuit of Fig. 27 shows a simple method of series connection of DF320 into the telephone set suitable for PABX or short line applications.

When the telephone handset is lifted C_1 is charged via D_1 to $(V_{Z1} - 0.7)$ volts and DF320 power on reset occurs. When the first keyed digit is recognised M1 goes to logic "1" muting the telephone network by switching on the low ON resistance JFET T_1, and maximising the line loop current for impulsing. Impulsing occurs through DP switching T_2 and hence T_3 off. Rapid discharge of C_1 through Z_1 is prevented during line break by the blocking diode D_1.

When dialling is complete the circuit returns to the static standby condition and T_1 is switched off. Circuit reset during a line interruption by the cradle switch is as for the parallel connection mode.

If a requirement exists that no semiconductor components should appear in the telephone loop during normal speech, the circuit of Fig. 28 is required.

Whilst the circuits of Figs. 26 and 27 did not require a common keyboard contact, it is necessary to have a common changeover switch in this case operating in conjunction with a bistable relay. In this application external control of CE is provided by the R_1, C_2 network. If, when the handset is lifted, the relay contact is such that the DF320 network is connected in circuit, it is necessary to initialise this relay to re-connect the telephone

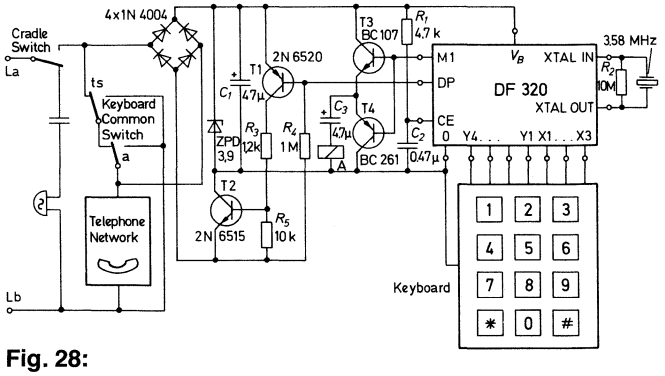


Fig. 28:
DF320 Bistable Relay Telephone Connection

network. This is achieved by the single pulse which occurs on M1 if CE goes to logic "1" in the absence of a keyboard input (Fig. 24).

When the first digit is keyed, the DF320 network is connected into the telephone loop and the telephone network short circuited by the keyboard common switch. M1 then goes to logic "1" switching the bistable relay hence maintaining the DF320 network in circuit. Impulsing occurs through DP switching T_1 off which in turn switches T_2. When dialling is complete the bistable relay is pulsed, switching the telephone network back in circuit and short circuiting the DF320 network.

The circuit of Fig. 29 shows additional gating circuitry to provide an automatic access pause after the first digit is dialled, by controlling HOLD. This is useful in PABX applications, eliminating the need for a manual hold facility if RE-DIAL is used.

The basic interface circuit is similar to that shown in Fig. 27. Muting is achieved by T_3 and line switching by T_2 driven by T_1.

In the on-hook condition T_1 is held off by G_{13} and standby current is supplied to the DF320 network by R_8; Z_1 providing voltage limiting. CE is clamped to logic "0" by G_3. The DF320 is in the static standby mode and the previously dialled number is stored.

When the handset is lifted G_{13} goes to logic "0" switching T_1 and hence T_2 on. The DF320 network V_B is now given by $(V_{Z2} - 0.7)$ volts. The DF320 remains in the static standby mode until the first key operation. G_1 decodes the common key function toggling the latch formed by G_2 and G_3 causing CE = "1". CE remains at logic "1" throughout the remainder of the off-hook condition ensuring that all digits keyed are stored by the DF320 as one number string (see FUNCTIONAL DESCRIPTION, DATA ENTRY).

If the first key operated is RE-DIAL, this condition is decoded by G_5, and via G_6 sets the latch formed by G_7 and G_8. G_9 is enabled and the first dial pulse causes the latch formed by G_{11} and G_{12} to be set taking HOLD to logic "1". When the first digit is complete M1 goes to logic "0" enabling the telephone network. When dial tone is recognised the CONTINUE switch is operated causing HOLD = "0" by resetting the latches formed by G_{11}, G_{12} and G_7, G_8. The remainder of the number is then re-dialled. Subsequent operation of RE-DIAL is blocked by G_6.

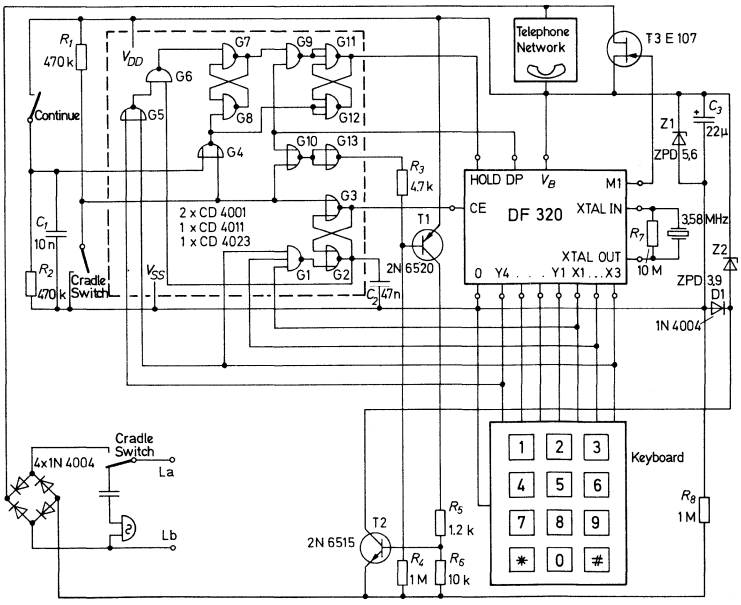


Fig. 29:
DF320 Series Telephone Connection
Re-Dial with automatic single digit access pause for PABX

Fig. 30 shows a simple method of interfacing a single contact matrix-type keyboard to the DF320 (DF321, DF322, DF323). Operation of a key causes the on-chip pull-up transistor of the Y input to provide base drive current to the corresponding X input external bipolar transistor, which sinks the X input pull-up current through its collector. Hence, a valid code is presented.

As an alternative to the crystal oscillator it is possible to operate the DF320 (DF321, DF322, DF323) from an LC combination connected as shown in Fig. 31. F01 is connected to V_{DD} selecting the 932 Hz impulsing condition. An oscillator frequency of 38.4 kHz will give a 10 Hz impulsing rate.

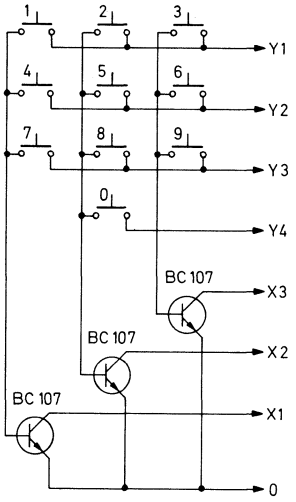


Fig. 30:
Single contact keyboard interface

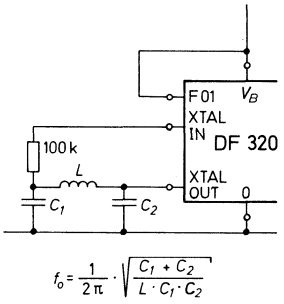


Fig. 31:
LC Oscillator

4096-Bit Dynamic Random Access Memory

Features

- Industry standard 16 pin DIP
- 150 ns access time (ITT 4027–2)
- 200 ns access time (ITT 4027–3)
- 250 ns access time (ITT 4027–4)
- 350 ns access time (ITT 4027–6)
- All inputs including clocks are TTL compatible
- Standard power supplies, +12V, +5V, –5V with ± 10% tolerance
- Three state TTL compatible output. Data out is latched and valid into next cycle.
- Page mode capability
- Adresses, chip select and data in have on-chip latches.
- Pin and function compatible with Mostek MK 4027

General

The ITT 4027 is a 4096 word by one bit random access memory fabricated with ITT's coplanar silicon gate process for high performance and high functional density. A single transistor dynamic storage cell and dynamic balanced sense amplifiers as used in the ITT 4027 achieve high speed with low power dissipation.

Packaging of the ITT 4027 in the industry standard 16 pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the ITT 4027 on 6 address input pins. Two TTL clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$) latch the two 6 bit address words into the ITT 4027. The 16 pin DIP gives the highest system bit densities and can be handled with widely available automatic testing and insertion equipment.

Several operating modes are incorporated in the ITT 4027 in addition to the usual read and write cycles: read modify write, page mode and $\overline{RAS}$ only refresh cycles are available.

The ITT 4027 is pin and function compatible with all popular 16 pin dynamic random access memories such as the MK 4096, MK 4027, and the Intel 2104 with the addition of superior system performance.

Absolute Maximum Ratings*

Voltage on any pin relative to V_{BB}	–0.5 V to +20 V
Voltage on V_{DD}, V_{CC} relative to V_{SS}	–1.0 V to +15 V
$V_{BB} - V_{SS}$ ($V_{DD} - V_{SS} > 0V$)	0 V
Operating temperature, T_A (Ambient)	0 °C to +70 °C
Storage temperature (Ambient)	–65 °C to +150 °C
Short circuit output current	50 mA
Power dissipation	1 Watt

* Exposure to absolute maximum conditions for extended periods may affect device reliability.

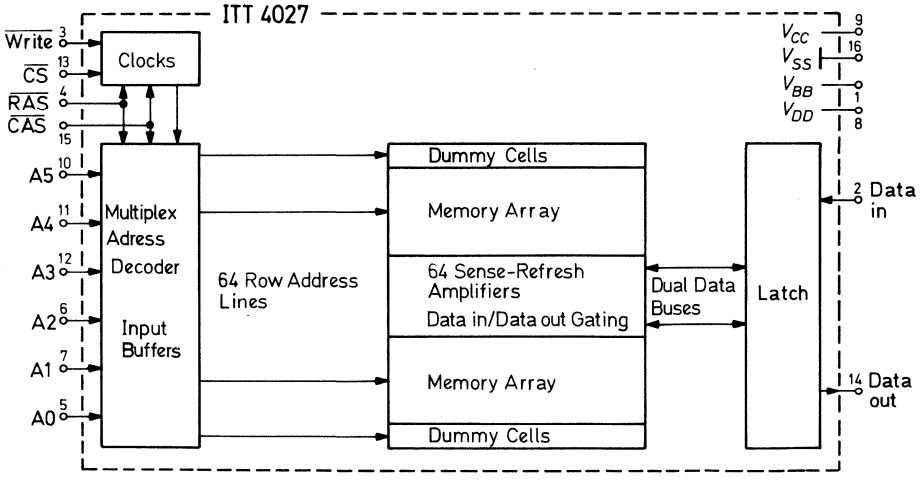


Fig. 1: Block Diagram

Package Description

The ITT 4027 is available in two different package versions:

- in a cerdip 16 pin glass sealed ceramic package, weight approx. 2 g, suffix D to the type number
- in a 16 pin plastic package, weight approx. 1.2 g, suffix N to the type number

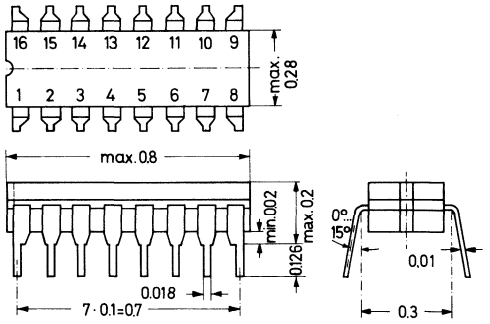


Fig. 2a: Cerdip Package (Sufix D)

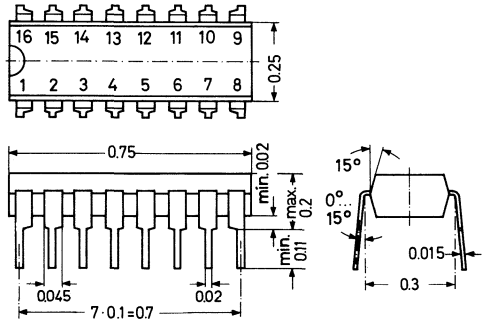


Fig. 2b: Plastic Package (Suffix N)

All Dimensions in inches

Pin Connections

1	Supply voltage V_{BB}	9	Supply voltage V_{CC}
2	Input Data in	10	Adress input A_5
3	$\overline{WRITE}$ input	11	Adress input A_4
4	$\overline{RAS}$ input	12	Adress input A_3
5	Address input A_0	13	$\overline{CS}$ input
6	Address input A_2	14	Output data out
7	Address input A_1	15	$\overline{CAS}$ input
8	Supply voltage V_{DD}	16	Supply voltage V_{SS}

Recommended DC Operating Conditions ($0\,°C \leq T_A \leq 70\,°C$)[1]

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{DD}	10.8	12.0	13.2	volts	2
Supply Voltage	V_{CC}	4.5	5.0	5.5	volts	2,3
Supply Voltage	V_{SS}	0	0	0	volts	2
Supply Voltage	V_{BB}	–4.5	–5.0	–5.5	volts	2
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$						
ITT4027-2	V_{IHC}	2.4	–	7.0	volts	2
ITT4027-3	V_{IHC}	2.4	–	7.0	volts	2
ITT4027-4	V_{IHC}	2.4	–	7.0	volts	2
ITT4027-6	V_{IHC}	2.7	–	7.0	volts	2
Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$						
ITT4027-2	V_{IH}	2.7	–	7.0	volts	2
ITT4027-3	V_{IH}	2.2	–	7.0	volts	2
ITT4027-4	V_{IH}	2.2	–	7.0	volts	2
ITT4027-6	V_{IH}	2.4	–	7.0	volts	2
Logic 0 Voltage, all inputs	V_{IL}	–1.0	–	0.8	volts	2

DC Electrical Characteristics[4] ($0\,°C \leq T_A \leq 70\,°C$)[1] ($V_{DD} = 12\,V \pm 10\%$; $V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$; $V_{BB} = -5\,V \pm 10\%$)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Average V_{DD} Power Supply Current	I_{DD1}	–	–	35	mA	5
Standby V_{DD} Power Supply Current	I_{DD2}	–	–	2	mA	8
Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles	I_{DD3}	–	–	25	mA	–
V_{CC} Power Supply Current	I_{CC}	–	–	–	mA	6
Average V_{BB} Power Supply Current	I_{BB}	–	–	150	µA	–
Input Leakage Current (any input)	I_{IL}	–	–	10	µA	7
Output Leakage Current	I_{OL}	–	–	10	µA	8,9
Output Logic 1 Voltage at $I_{OUT} = -5\,mA$	V_{OH}	2.4	–	–	volts	–
Output Logic 0 Voltage at $I_{OUT} = 3.2\,mA$	V_{OL}	–	–	0.4	volts	–

AC Electrical Characteristics ($0\,°C \leq T_A \leq 70\,°C$) ($V_{DD} = 12\,V \pm 10\%$; $V_{SS} = 0\,V$; $V_{BB} = -5\,V \pm 10\%$)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Input Capacitance (A_0-A_5), D_{IN}, $\overline{CS}$	C_{I1}	–	4	5	pF	10
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	–	8	10	pF	10
Output Capacitance (D_{OUT})	C_O	–	5	7	pF	8,10

Electrical Characteristics and Recommended AC Operating Conditions (Notes 4, 11, 17)

(0 °C ≤ T_A ≤ 70 °C)[1] (V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{SS} = 0V, V_{BB} = –5V ±10%)

Parameter	Symbol	4027–2		4027–3		4027–4		4027–6			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units	Notes
Random read or write cycle time	t_{RC}	320	–	375	–	375	–	500	–	ns	12
Read write cycle time	t_{RWC}	330	–	420	–	480	–	700	–	ns	12
Access time from row address strobe	t_{RAC}	–	150	–	200	–	250	–	350	ns	13,15
Access time from column address strobe	t_{CAC}	–	100	–	135	–	165	–	200	ns	14,15
Output buffer turn-off delay	t_{OFF}	–	40	–	50	–	60	–	100	ns	–
Row address strobe precharge time	t_{RP}	100	–	120	–	120	–	150	–	ns	–
Row address strobe pulse width	t_{RAS}	150	10,000	200	10,000	250	10,000	350	10,000	ns	–
Row address strobe hold time	t_{RSH}	100	–	135	–	165	–	200	–	ns	–
Column address strobe pulse width	t_{CAS}	100	–	135	–	165	–	200	–	ns	–
Row to column strobe delay	t_{RCD}	20	50	25	65	35	85	100	140	ns	16
Row address set-up time	t_{ASR}	0	–	0	–	0	–	0	–	ns	–
Row address hold time	t_{RAH}	20	–	25	–	35	–	100	–	ns	–
Column address set-up time	t_{ASC}	–10	–	–10	–	–10	–	0	–	ns	–
Column address hold time	t_{CAH}	45	–	55	–	75	–	100	–	ns	–
Column address hold time referenced to $\overline{RAS}$	t_{AR}	95	–	120	–	160	–	250	–	ns	–
Chip select set-up time	t_{CSC}	–10	–	–10	–	–10	–	0	–	ns	–
Chip select hold time	t_{CH}	45	–	55	–	75	–	100	–	ns	–
Chip select hold time referenced to $\overline{RAS}$	t_{CHR}	95	–	120	–	160	–	250	–	ns	–
Transition time (rise and fall)	t_T	3	35	3	50	3	50	3	50	ns	17
Read command set-up time	t_{RCS}	0	–	0	–	0	–	0	–	ns	–
Read command hold time	t_{RCH}	0	–	0	–	0	–	0	–	ns	–
Write command hold time	t_{WCH}	45	–	55	–	75	–	150	–	ns	–
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	95	–	120	–	160	–	300	–	ns	–
Write command pulse width	t_{WP}	45	–	55	–	75	–	150	–	ns	–
Write command to row strobe lead time	t_{RWL}	50	–	70	–	85	–	150	–	ns	–
Write command to column strobe lead time	t_{CWL}	50	–	70	–	85	–	150	–	ns	–
Data in set-up time	t_{DS}	0	–	0	–	0	–	0	–	ns	18
Data in hold time	t_{DH}	45	–	55	–	75	–	150	–	ns	18
Data in hold time referenced to $\overline{RAS}$	t_{DHR}	95	–	120	–	160	–	300	–	ns	–
Column to row strobe precharge time	t_{CRP}	0	–	0	–	0	–	50	–	ns	–
Column precharge time	t_{CP}	60	–	80	–	110	–	150	–	ns	–
Refresh period	t_{RFSH}	–	2	–	2	–	2	–	2	ms	–
Write command set-up time	t_{WCS}	0	–	0	–	0	–	0	–	ns	19
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	60	–	80	–	90	–	200	–	ns	19
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	110	–	145	–	175	–	300	–	ns	19
Data out hold time	t_{DOH}	10	–	10	–	10	–	10	–	µs	–

Notes

1. T_A is specified for operation at frequencies $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met.

2. All voltages referenced to V_{SS}.

3. Output Voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

4. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

5. Current is proportional to cycle rate. I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min).

6. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to Data out. At all other times I_{CC} consists of leakage currents only.

7. All device pins at 0 volts except V_{BB} which is at –5 volts and the pin under test which is at +10 volts.

8. Output is disabled (high impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.

9. $0\,V \leq V_{OUT} \leq +10\,V$

10. Effective capacitance is calculated from the equation:
$C = \frac{\triangle Q}{\triangle V}$ with $\triangle V = 3$ volts

11. A. C. measurements assume $t_T = 5$ ns

12. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0\,°C \leq T_A \leq 70\,°C$) is assured.

13. Assumes that $t_{RCD} \leq t_{RCD}$ (max)

14. Assumes that $t_{RCD} \geq t_{RCD}$ (max)

15. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

16. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

17. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

18. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

19. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$ (min), and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

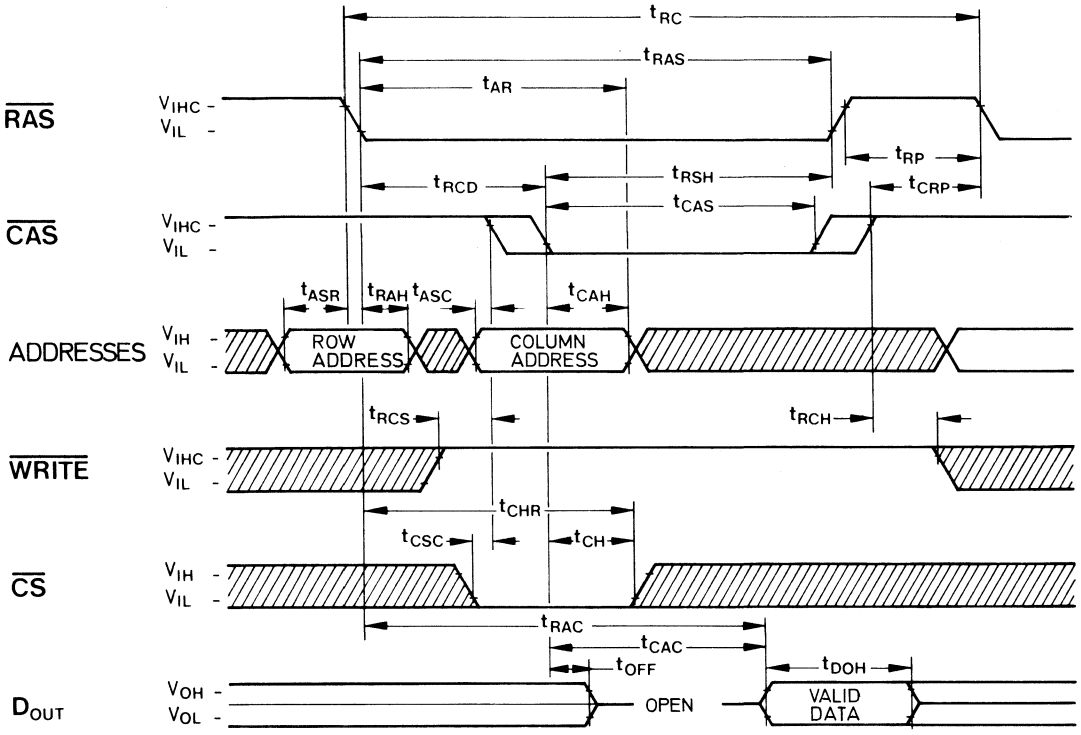


Fig. 3: Read cycle

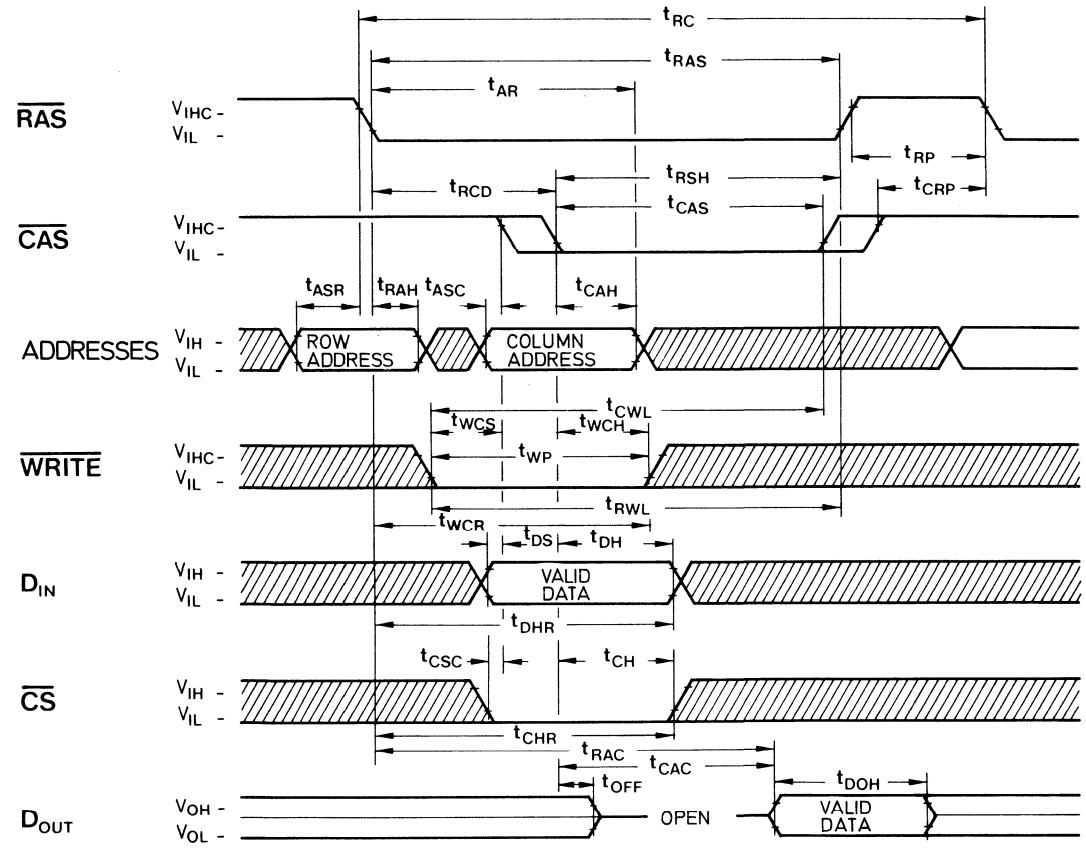


Fig. 4: Write cycle

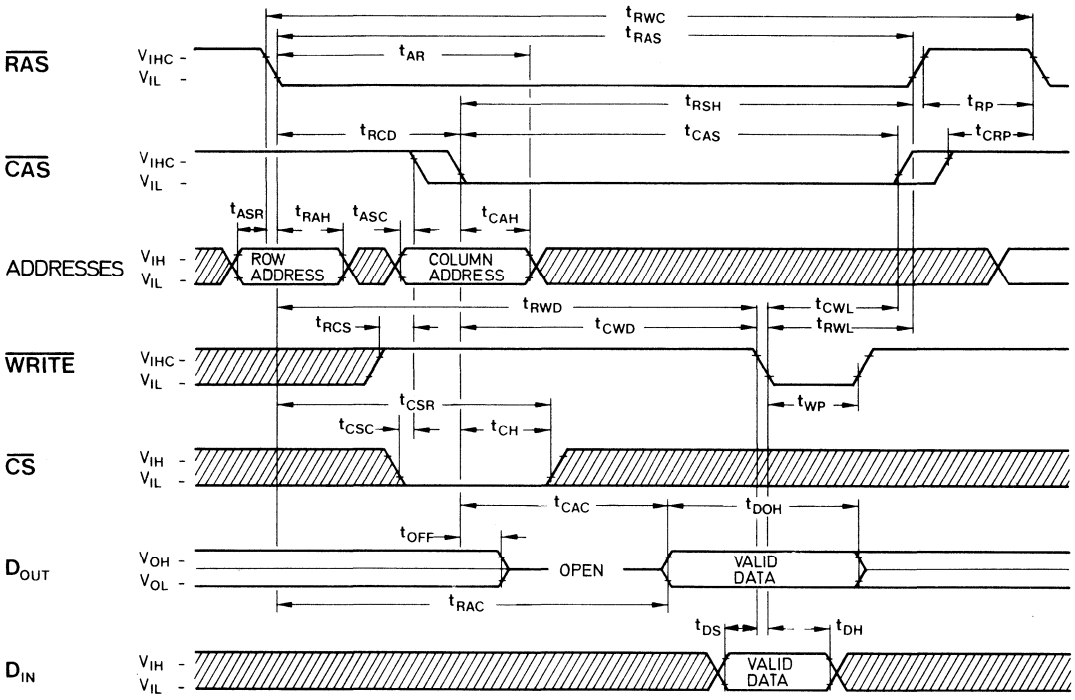


Fig. 5: Read–Write/Read–Modify–Write cycle

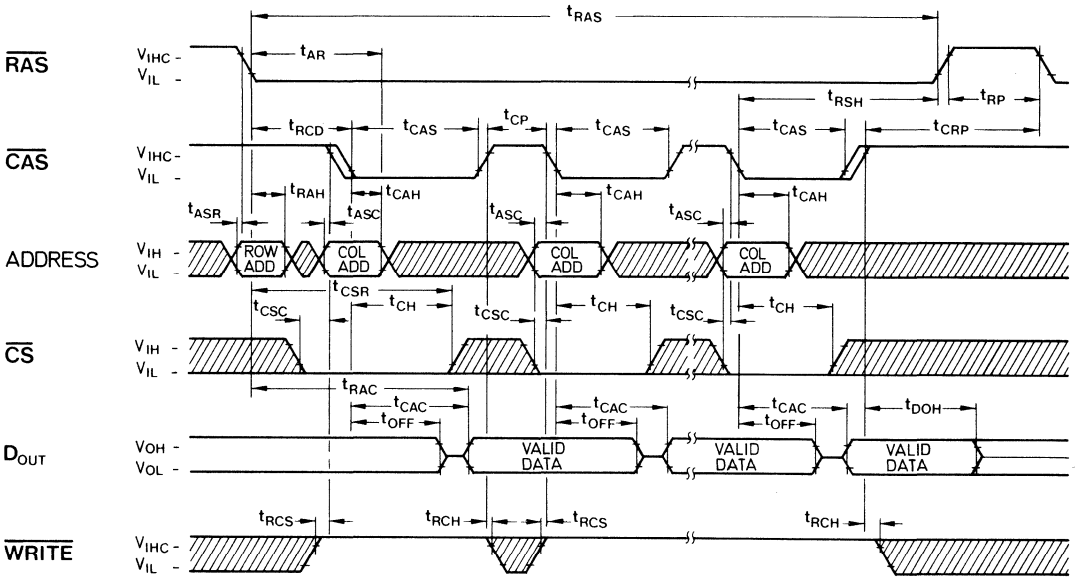


Fig. 6: Page mode read cycle

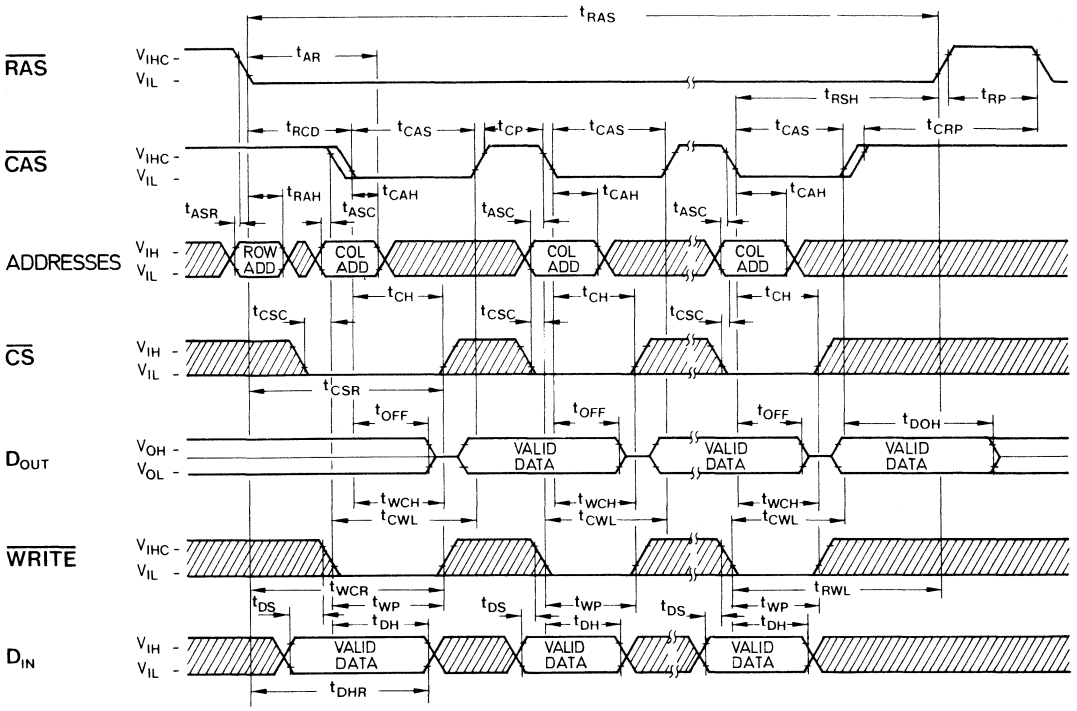


Fig. 7: Page mode write cycle

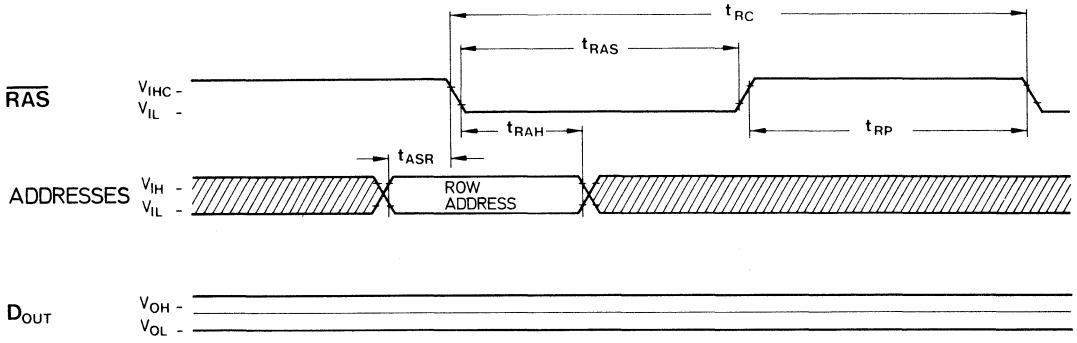


Fig. 8: "$\overline{\text{RAS}}$ only" refresh cycle. Note: D_{OUT} remains unchanged from previous cycle.

Addressing

The 12 address bits required to decode 1 of the 4096 cell locations within the ITT 4027 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by two negative-going TTL clock pulses. The first clock, Row Address Strobe ($\overline{RAS}$), latches the six row address bits into the chip. The second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits together with the Chip Select ($\overline{CS}$) into the chip.

The column information can be applied to the chip before it is actually required. Therefore, the hold time requirements for the input signal associated with $\overline{CAS}$ are also referenced to $\overline{RAS}$. This gated $\overline{CAS}$ feature helps the system designer allow for timing skews that may arise in multiplexing operations.

Since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle, its decoding time does not add to system access or cycle time.

Data Input/Output

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the $\overline{WRITE}$ or $\overline{CAS}$ signals to make a negative transition ist the strobe for the Data In Register. This permits several options in the write cycle timing. In a write cycle if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is preferred that the cycle be a read-write cycle, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. To show this, Data In is referenced to the negative edge of $\overline{WRITE}$ in the timing diagram for the read-write and page mode write cycles, wehreas the "early write cycle" diagram shows Data In referenced to $\overline{CAS}$.

Note that if the chip is unselected, that is with $\overline{CS}$ high at $\overline{CAS}$ time, the $\overline{WRITE}$ commands are not executed and consequently data stored in the memory is unchanged.

Data is retrieved from the memory in a read cycle by holding $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will then be available at the output within the specified access time.

Data Output Latch

A change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ signal. The output buffer is not affected by memory cycles in which only the $\overline{RAS}$ signal is applied to the ITT 4027. Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open circuit, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will go active at the access time and contain the data read from the selected cell; this data is the same polarity as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ going low prior to $\overline{CAS}$ going low) and the chip is selected, then at the access time the output latch and buffer will contain the input data. Having become active, the output will remain valid until the ITT 4027 receives the next $\overline{CAS}$ negative edge. Any further refresh cycles in which $\overline{RAS}$ is received (but no $\overline{CAS}$) will not cause the valid data to be affected. Conversely, the output will assume the open-circuit state in any cycle in which the ITT 4027 receives a $\overline{CAS}$ but no $\overline{RAS}$ signal (regardless of the state of any ohter inputs. The output will also assume the open circuit state in normal cycles which $\overline{RAS}$ and $\overline{CAS}$ signals occur if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logical 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135 Ω typically. The resistance to V_{SS} (logic 0 state) is 125 Ω maximum and 50 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation the power may be removed from the V_{CC} pin without affecting the ITT 4027 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

Refresh

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a $\overline{RAS}$ signal occurs accomplishes a refresh operation. A read cycle will refresh the selected row regardless of the state of the Chip Select $\overline{CS}$ input. A write or read-modify-write cycle also refreshes the selected row, however the chip should be unselected to prevent data being written into the selected cell. If, during a refresh cycle, the ITT 4027 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. However, if $\overline{RAS}$ only refresh cycles, that is where $\overline{RAS}$ is the only signal applied to the chip, are continued for long periods, the output buffer may eventually lose proper data and go open circuit. The output buffer will regain activity during the first cycle in which the $\overline{CAS}$ is applied to the Chip.

Power Dissipation/Standby Mode

Most of the circuitry used in the ITT 4027 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 170 mW at 1 μs cycle rate for the ITT 4027 with a worst case power of less than 470 mW at 375 ns cycle time. To minimize the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a $\overline{RAS}$, however, will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs. If the $\overline{RAS}$ signal is decoded and supplied only to the selected chips, then the Chip Select ($\overline{CS}$) input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited)

regardless of the Chip Select input. For refresh cycles, however, either the $\overline{CS}$ input of all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-ORed" outputs from turning on with opposing force. Note that the ITT 4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ memory cycle.

Page Mode Operation

The "Page Mode" feature of the ITT 4027 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and keeping the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. The "page mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. The chip select input ($\overline{CS}$) is operative in page mode cycles just as in normal cycles. It is not necessary that the chip be selected during the first operation in a sequence of page cycles. Likewise, the $\overline{CS}$ input can be used to select or disable any cycle(s) in a series of page cycles. This feature allows the page boundary to be extended beyond the 64 column locations in a single chip. The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and decoding $\overline{CS}$ to select the required block. The ITT 4027 – 6 is designed primarily as a replacement for first generation 4K dynamic random access memories, such as the Mostek MK 4096–11 and the Intel 2104 which are not designed for page mode operation; therefore the ITT 4027–6 is not specified to operation in this mode.

Power Up

The ITT 4027 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to ensure compliance with the Absolute Maximum Ratings, ITT recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and Data Out to the inactive state.

After power is applied to the device, the ITT 4027 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

16384-Bit Dynamic Random Access Memory

Features

- Industry standard 16 pin DIP
- 150 ns access time (ITT 4116–2)
- 200 ns access time (ITT 4116–3)
- 250 ns access time (ITT 4116–4)
- All inputs including clocks are TTL compatible
- Standard power supplies, +12V, +5V, −5V with ± 10% tolerance
- Three state TTL compatible output, Data out is not latched
- Page mode capability
- Addresses and data in have on-chip latches
- Pin and function compatible with Mostek MK 4116

General

The ITT 4116 is a 16384 word by one bit random access memory fabricated with ITT's N-channel double-poly coplanar silicon gate process for high performance and high functional density. A single transistor dynamic storage cell and dynamic balanced sense amplifiers as used in the ITT 4116 achieve high speed with low power dissipation.

Packaging of the ITT 4116 in the industry standard 16 pin package is made possible by multiplexing the 14 address bits (required to address 1 of 16384 bits) into the ITT 4116 on 7 address input pins (A_0-A_6). Two TTL clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), latch the two 7 bit address words into the ITT 4116. The 16 pin DIP gives the highest system bit densities and can be handled with widely available automatic testing and insertion equipment.

Several operating modes are incorporated in the ITT 4116 in addition to the usual read and write cycles; read modify write, page mode and $\overline{RAS}$ only refresh cycles are available.

The ITT 4116 16384 bit memory has the same pin layout as the industry standard ITT 4027 4096 bit memory with the exception of chip select which is replaced by an additional address input needed to accommodate 16384 bits.

Absolute Maximum Ratings*

Voltage on any pin relative to V_{BB}	−0.5V to +20V
Voltage on V_{DD}, V_{CC} relative to V_{SS}	−1.0V to +15V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS}>0$)	0V
Operating temperature, T_A (Ambient)	0°C to +70°C
Storage temperature (Ambient)	−65°C to +150°C
Short Circuit Output Current	50mA
Power dissipation	1Watt

* Exposure to absolute maximum conditions for extended periods may affect device reliability.

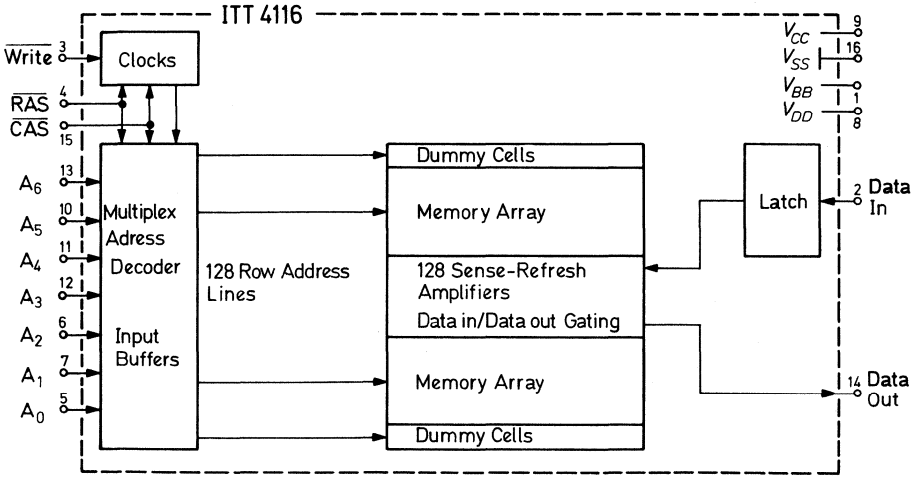


Fig. 1: Block Diagram

Package Description

The ITT 4116 is available in two different package versions:

- in a cerdip 16 pin glass sealed ceramic package, weight approx. 2 g, suffix D to the type number
- in a 16 pin plastic package, weight approx. 1.2 g, suffix N to the type number

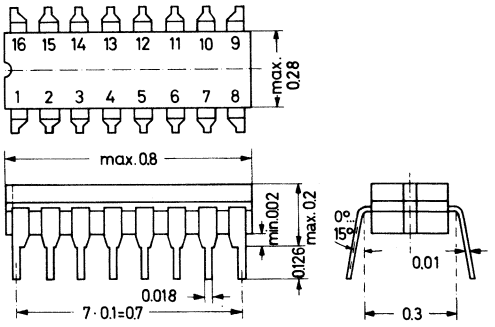


Fig. 2a: Cerdip Package (Suffix D)

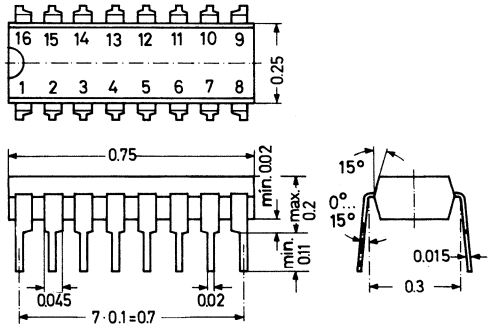


Fig. 2b: Plastic Package (Suffix N)

All Dimensions in inches

Pin Connections

1	Supply Voltage V_{BB}	9	Supply voltage V_{CC}
2	Input Data in	10	Address input A_5
3	$\overline{WRITE}$ input	11	Address input A_4
4	$\overline{RAS}$ input	12	Address input A_3
5	Address input A_0	13	Address input A_6
6	Address input A_2	14	Output Data out
7	Address input A_1	15	$\overline{CAS}$ input
8	Supply voltage V_{DD}	16	Supply voltage V_{SS}

Recommended DC Operating Conditions[4] ($0\ °C \leq T_A \leq 70\ °C$)[1]

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{DD}	10.8	12.0	13.2	volts	2
Supply Voltage	V_{CC}	4.5V	5.0	5.5	volts	2,3
Supply Voltage	V_{SS}	0	0	0	volts	2
Supply Voltage	V_{BB}	–4.5	–5.0	–5.7	volts	2
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7	–	7.0	volts	2
Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.4	–	7.0	volts	2
Logic 0 Voltage, all inputs	V_{IL}	–1.0	–	0.8	volts	2

DC Electrical Characteristics[4] ($0\ °C \leq T_A \leq 70\ °C$)[1] ($V_{DD} = 12\ V \pm 10\%$; $V_{CC} = 5\ V \pm 10\%$; $V_{SS} = 0\ V$; $V_{BB} = -4.5\ V$ to $-5.7\ V$)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Operating Current						
Average power supply operating current	I_{DD1}	–	–	35	mA	5
$\overline{RAS}$, $\overline{CAS}$ cycling: $t_{RC} = t_{RC}$ (min)	I_{CC1}	–	–	–	–	6
	I_{BB1}	–	–	200	µA	–
Standby current						
Power supply standby current	I_{DD2}	–	–	1.5	mA	18
($\overline{RAS} = V_{IHC}$)	I_{CC2}	–10	–	10	µA	–
	I_{BB2}	–	–	100	µA	–
Refresh Current						
Average power supply current,	I_{DD3}	–	–	27	mA	5, 18
refresh mode	I_{CC3}	–10	–	10	µA	–
($\overline{RAS}$ cycling, $t_{RC} = t_{RC}$ (min)	I_{BB3}	–	–	200	µA	–
Page Mode Current						
Average power supply current,	I_{DD4}	–	–	27	mA	5
page mode operation	I_{CC4}	–	–	–	–	6
($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}$ (min)	I_{BB4}	–	–	200	µA	–
Input Leakage Current any input ($V_{BB} = -5\ V$, $0\ V \leq V_{IN} \leq +7.0\ V$, all other pins not under test = 0 volts)	I_{IL}	–10	–	10	µA	–
Output Leakage Current	I_{OL}	–10	–	10	µA	18, 19
Output Levels						
Output high (Logic 1) voltage ($I_{OUT} = -5$ mA)	V_{OH}	2.4	–	–	volts	3
Output low (Logic 0) voltage ($I_{OUT} = 4.2$ mA)	V_{OL}	–	–	0.4	volts	–

AC Electrical Characteristics ($0\,°C \leq T_A \leq 70\,°C$) ($V_{DD} = 12.0\,V \pm 10\%$; $V_{SS} = 0\,V$; $V_{BB} = -4.5\,V$ to $-5.7\,V$)

Parameter	Symbol	Typ.	Max.	Units	Notes
Input Capacitance (A_0–A_6), D_{IN}	C_{11}	4	5	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{12}	8	10	pF	17
Output Capacitance (D_{OUT})	C_O	5	7	pF	17,18

Electrical Characteristics and Recommended AC Operating Conditions (Notes 4, 7, 11)

($0\,°C \leq T_A \leq 70\,°C$)[1] ($V_{DD} = 12.0\,V \pm 10\%$; $V_{CC} = 5.0\,V \pm 10\%$; $V_{SS} = 0\,V$, $V_{BB} = -4.5\,V$ to $-5.7\,V$)

Parameter	Symbol	ITT 4116-2		ITT 4116-3		ITT 4116-4			
		Min.	Max.	Min.	Max.	Min.	Max.	Units	Notes
Random read or write cycle time	t_{RC}	320	–	375	–	410	–	ns	8
Read write cycle time	t_{RWC}	320	–	375	–	425	–	ns	8
Read modify write cycle time	t_{RMW}	320	–	405	–	500	–	–	–
Page mode cycle time	t_{PC}	170	–	225	–	275	–	ns	–
Access time from $\overline{RAS}$	t_{RAC}	–	150	–	200	–	250	ns	9,12
Access time from $\overline{CAS}$	t_{CAC}	–	100	–	135	–	165	ns	10,12
Output buffer turn-off delay	t_{OFF}	0	40	0	50	0	60	ns	13
Transition time (rise and fall)	t_T	3	35	3	50	3	50	ns	7
$\overline{RAS}$ precharge time	t_{RP}	100	–	120	–	150	–	ns	–
$\overline{RAS}$ pulse width	t_{RAS}	150	10,000	200	10,000	250	10,000	ns	–
$\overline{RAS}$ hold time	t_{RSH}	100	–	135	–	165	–	ns	–
$\overline{CAS}$ hold time	t_{CSH}	150	–	200	–	250	–	ns	–
$\overline{CAS}$ pulse width	t_{CAS}	100	–	135	–	165	–	ns	–
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	65	35	85	ns	14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	–20	–	–20	–	–20	–	ns	–
Row Address set-up time	t_{ASR}	0	–	0	–	0	–	ns	–
Row Address hold time	t_{RAH}	20	–	25	–	35	–	ns	–
Column Address set-up time	t_{ASC}	–10	–	–10	–	–10	–	ns	–
Column Address hold time	t_{CAH}	45	–	55	–	75	–	ns	–
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	95	–	120	–	160	–	ns	–
Read command set-up time	t_{RCS}	0	–	0	–	0	–	ns	–
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	–
Write command hold time	t_{WCH}	45	–	55	–	75	–	ns	–
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	95	–	120	–	160	–	ns	–
Write command pulse width	t_{WP}	45	–	55	–	75	–	ns	–
Write command to $\overline{RAS}$ lead time	t_{RWL}	50	–	70	–	85	–	ns	–
Write command to $\overline{CAS}$ lead time	t_{CWL}	50	–	70	–	85	–	ns	–
Data-in set-up time	t_{DS}	0	–	0	–	0	–	ns	15
Data-in hold time	t_{DH}	45	–	55	–	75	–	ns	15
Date-in hold time referenced to $\overline{RAS}$	t_{DHR}	95	–	120	–	160	–	ns	–
$\overline{CAS}$ precharge time (for page-mode cycle only)	t_{CP}	60	–	80	–	100	–	ns	–
Refresh period	t_{REF}	–	2	–	2	–	2	ms	–
$\overline{WRITE}$ command set-up time	t_{WCS}	–20	–	–20	–	–20	–	ns	16
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	60	–	80	–	90	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	110	–	145	–	175	–	ns	16

Notes

1. T_A is specified for operation at frequencies $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met.

2. All voltages referenced to V_{SS}.

3. Output Voltage will swing from V_{SS} to V_{CC} when enabled, with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

4. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

5. Current is proportional to cycle rate. I_{DD1} (max), I_{DD3} (max) and I_{DD4} are measured at the cycle rate specified by t_{RC} (min).

6. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to Data out. At all other times I_{CC} consists of leakage currents only.

7. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

8. The specifications for t_{RC} (min) and t_{RWC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0 °C $\leq T_A \leq$ 70 °C) is assured.

9. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

10. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

11. AC measurements assume $t_T = 5$ ns.

12. Measured with a load equivalent to 2 TTL loads and 100 pF.

13. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

15. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify write cycles.

16. t_{WCS}, t_{WCD} and t_{RWD} are restrictive operating parameters in R·W and RMW cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the Data Out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the Data Out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the Data Out (at access time) is indeterminate.

17. Effective capacitance calculated from the equation
$C = \frac{I \cdot \triangle t}{\triangle V}$
with $\triangle V = 3$ volts and power supplies at nominal levels.

18. $\overline{CAS} = V_{IHC}$ to disable D_{OUT}.

19. $0\ V \leq V_{OUT} \leq +\ 5.5\ V$.

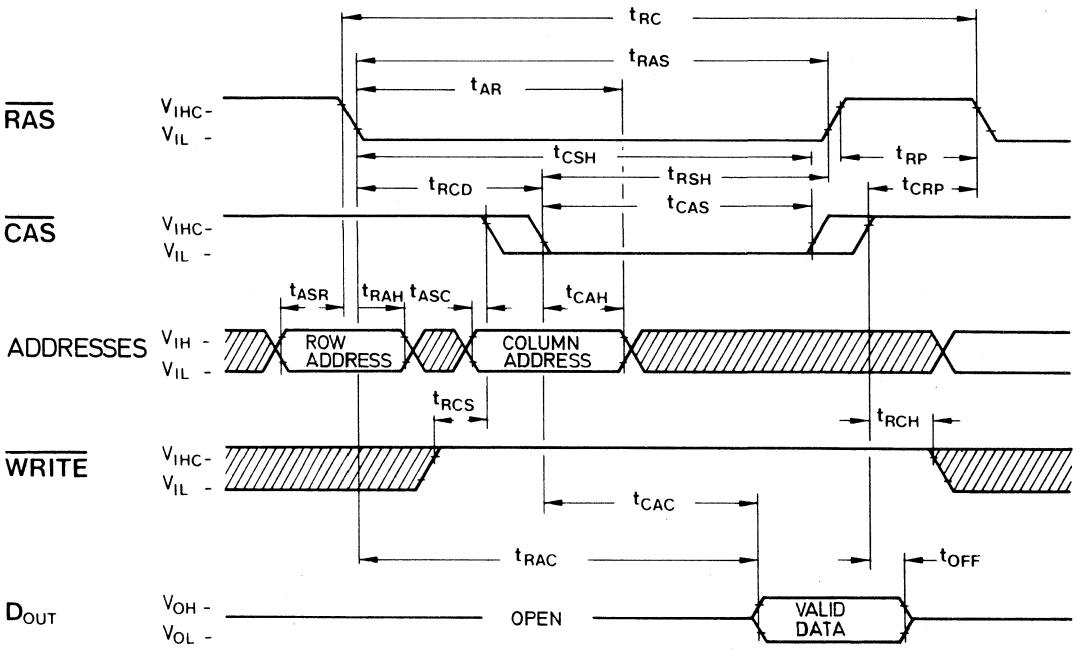


Fig. 3: Read Cycle

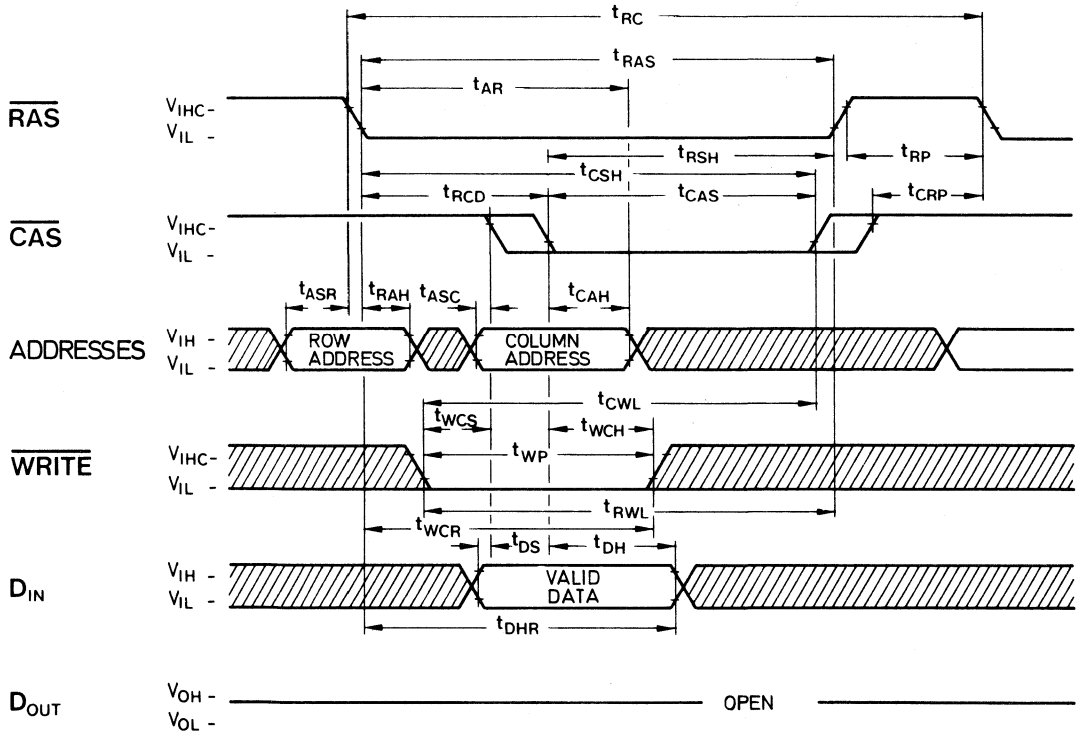


Fig. 4: Write Cycle (Early Write)

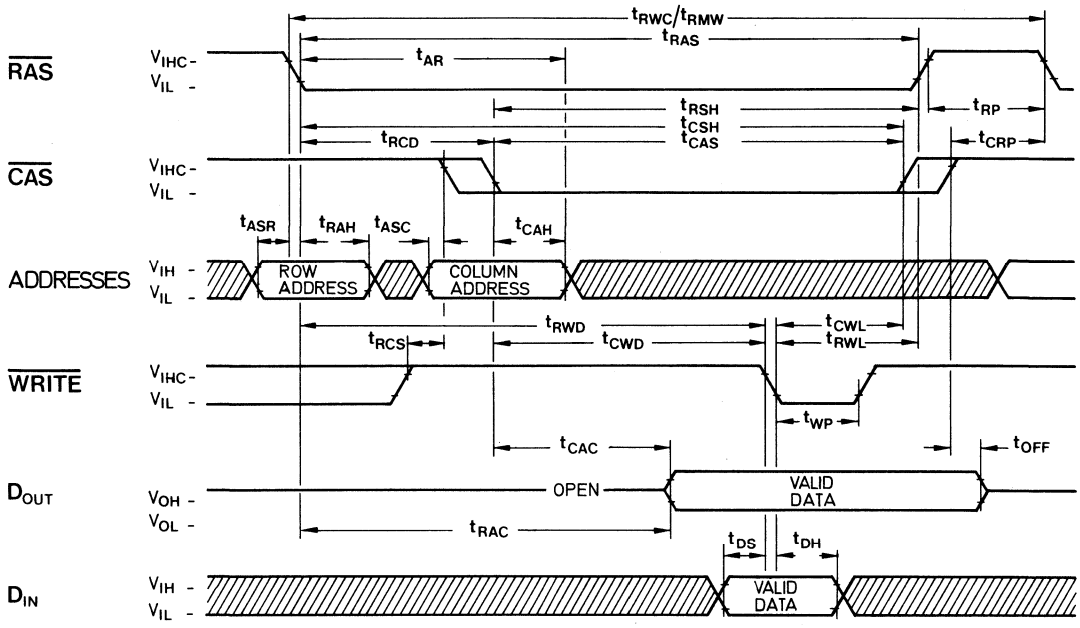


Fig. 5: Read–Write/Read–Modify–Write Cycle

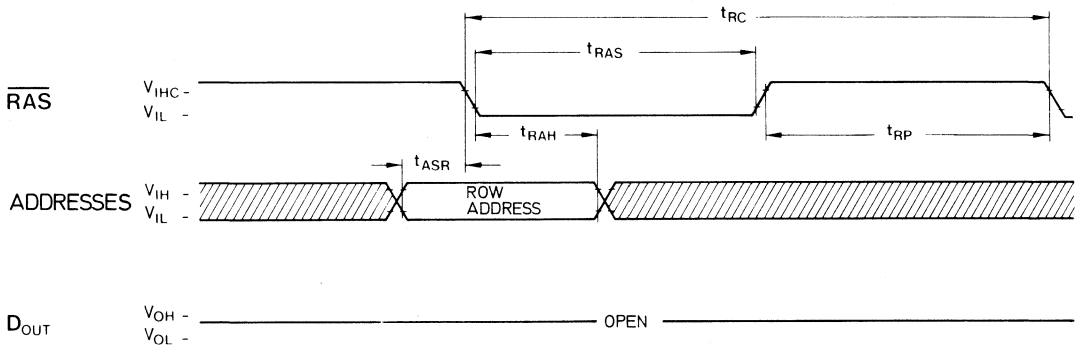


Fig. 6: "$\overline{\text{RAS}}$–Only" Refresh Cycle
Note: $\overline{\text{CAS}}$ = V_{IHC}, $\overline{\text{WRITE}}$ = Don't Care

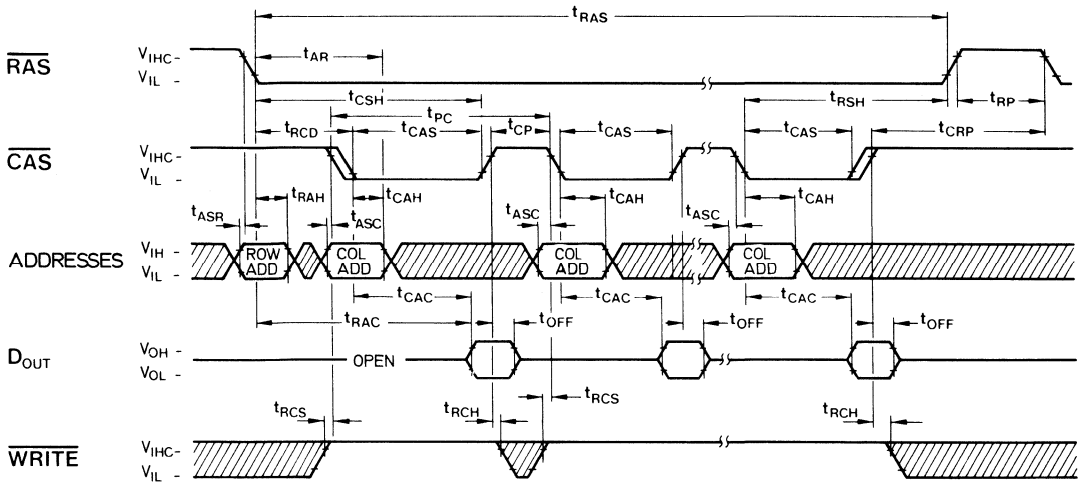


Fig. 7: Page Mode Read Cycle

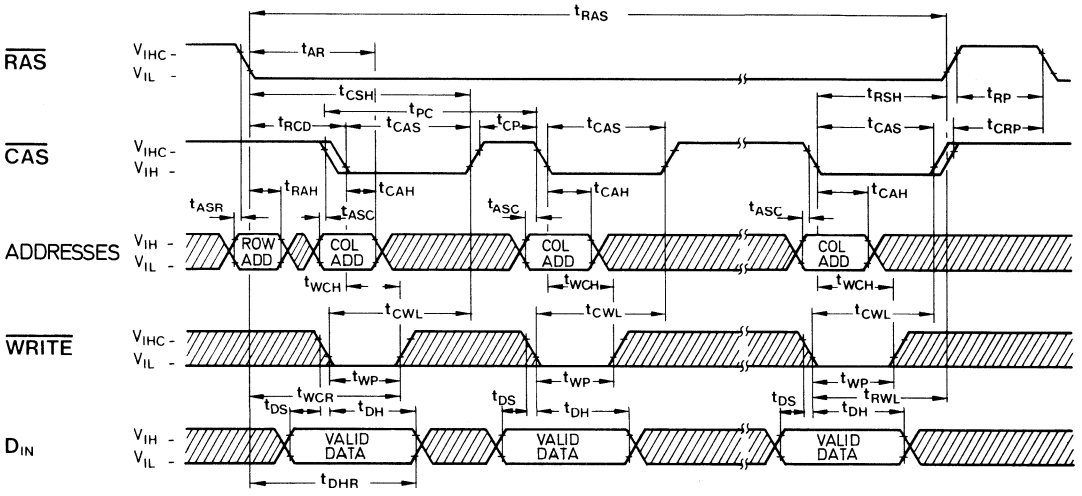


Fig. 8: Page Mode Write Cycle

Addressing

Fourteen address bits are necessary to decode 1 of the 16384 cell locations and these are multiplexed on to the seven address inputs of the ITT 4116. Two externally applied negative going TTL clock pulses latch these inputs into on-chip address latches. Row Address Strobe ($\overline{RAS}$), the first clock, latches the 7 row address bits, and then Column Address Strobe ($\overline{CAS}$), the 7 column address bits. An internal clock chain is triggered by $\overline{RAS}$ and another by $\overline{CAS}$; these two logically linked clock chains control the address multiplexing operation so that it occurs outside the critical path timing sequence for read data access. The "gated $\overline{CAS}$" feature, that is the internal inhibition of the $\overline{CAS}$ clock chain until the occurrence of a delayed signal from the $\overline{RAS}$ clock chain, allows the $\overline{CAS}$ clock pulse to be applied immediately the Row address information has been changed to Column address information provided the Row Address Hold Time (t_{RAH}) specification has been met. Any delay in applying $\overline{CAS}$ after t_{RAH} will not affect the worst case data access time (t_{RAC}) provided $\overline{CAS}$ occurs before the delayed signal from the $\overline{RAS}$ clock chain. This window for $\overline{CAS}$ with no delay in t_{RAC} is delineated by two timing endpoints t_{RCD} (min) and t_{RCD} (max). If $\overline{CAS}$ is applied after t_{RCD} (max), no data storage or reading errors will result; however, the access time will be determined from $\overline{CAS}$ access time t_{CAC} and therefore t_{RAC} will be increased by the amount that the actual t_{RCD} exceeds the endpoint t_{RCD} (max).

Data Input/Output

Input data for an addressed cell is latched into an on-chip register when the three negative clocks $\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$ are active. The strobe for the Data In (D_{IN}) register is the negative edge of either $\overline{CAS}$ or $\overline{WRITE}$, whichever is the later, thus permitting various write cycle timing options. If the $\overline{WRITE}$ edge occurs first, D_{IN} is strobed by $\overline{CAS}$ and set-up and hold times are referenced to $\overline{CAS}$. In the case of a read-write cycle or if the data is not available at $\overline{CAS}$, then the D_{IN} is strobed by the delayed $\overline{WRITE}$ edge and set-up and hold times are referenced to $\overline{WRITE}$. "Delayed write" is depicted in the read-write and page mode write cycle timing diagrams and "early write" in the write cycle diagram.

Output of data from an addressed cell is achieved within the specified access time whilst $\overline{WRITE}$ is held inactive or high during the period $\overline{CAS}$ is active.

Data Output Control

Data Output (D_{OUT}) of the ITT 4116 is tri-state TTL compatible and is normally high impedance (i.e. open-circuit and floating). During a read cycle, the output will turn on to either logic 1 or logic 0 at the access time when $\overline{CAS}$ is activated (low level). The valid output data will remain until $\overline{CAS}$ is taken high.

In the case of a read, read-modify-write, or delayed write cycle, D_{OUT} contains the data read from the addressed cell after the access time; this data is the same polarity (not inverted) as the input data. Having gone active the validity of data until $\overline{CAS}$ goes high is unaffected by the subsequent state of $\overline{RAS}$.

If the cycle is "early write" ($\overline{WRITE}$ active before $\overline{CAS}$) then D_{OUT} remains in the high impedance state throughout the cycle. The effect of this mode of operation is that the user can control the data output by the position of the $\overline{WRITE}$ edge during a write cycle and the pulse width of $\overline{CAS}$ during read.

Output control of this nature results in important system operations:

Common I/O operation:
D_{IN} can be connected directly to D_{OUT} giving a common I/O data bus, provided all write operations are in the "early write" mode.

Data Output Control:
D_{OUT} contains valid data during a read cycle from t_{CAC} until $\overline{CAS}$ goes inactive, this allows data to remain valid until the beginning of a subsequent cycle without increasing overall memory cycle time. Thus flexible $\overline{RAS}$ / $\overline{CAS}$ timing relationships are possible.

Chip Selection:
As D_{OUT} is not latched, $\overline{CAS}$ is not required to turn off the outputs of unselected devices. Two methods of chip select are possible by decoding $\overline{CAS}$ and/or $\overline{RAS}$. If both are decoded then a two dimensional chip select array is possible.

Extended Page Boundary:
In page mode operation, multiple column locations are accessed using the same row address in successive memory cycles. If $\overline{CAS}$ is decoded as a page cycle select signal, the page boundary can be extended beyond the 128 column locations of an individual chip.

Output Interfacing

The data output buffer has a low impedance to V_{CC}, 420 Ω maximum (135 Ω typically), for logic state "1" and a low impedance to V_{SS}, 95 Ω maximum (35 Ω typically), for logic state "0". Power to the output buffer can be supplied at the supply voltage of interfacing chips using the separate V_{CC} pin. In standby battery operation, refresh operation of the ITT 4116 is unaffected by removal of power to this separate V_{CC}, thus all system logic except $\overline{RAS}$ timing circuitry and the refresh address logic may be turned off, minimising power requirements.

Page Mode Operation

Multiple column locations may be accessed using the same row address in successive memory cycles; this page mode of operation of the ITT 4116 gives increased speed without increased power. Power is reduced as the $\overline{RAS}$ is kept active (logic "0") after the initial strobe on the first cycle so eliminating the power required on the negative edge of $\overline{RAS}$. Additionally, access and cycle times are reduced by the elimination of time required for strobing the new row.

A single ITT 4116 limits the page boundary to the 128 columns available; however, when more than 16K words are used in a system, the use of $\overline{CAS}$ as a chip select signal extends the page boundary. $\overline{RAS}$ is applied to all devices and $\overline{CAS}$ is decoded as a page cycle select signal: only those devices receiving both $\overline{RAS}$ and $\overline{CAS}$ will perform memory cycles.

Refresh

The dynamic cell matrix requires refresh within every 2 milliseconds at each of the 128 row addresses. Although any memory cycle will achieve this refresh, substantial power savings can easily be made by using $\overline{RAS}$-only cycles as can be seen from the I_{DD3} specification.

Power Considerations

The ITT 4116 consists mainly of dynamic circuitry and most power is consumed on address strobe edges. Power, therefore, is a function of operating frequency rather than active duty cycle. Additionally destruction of the device will not result from the clock inputs accidentally becoming grounded.

Provided supply voltages are within specification, no special power noise restrictions are necessary, although adequate decoupling should be provided to suppress high frequency transients to ensure optimum reliability and system performance. As the ITT 4116 draws very little DC power there is minimal need for large capacitors.

For systems requiring low power dissipation, it is necessary to reduce the operation frequency. For example, if the cycle time is 1 microsecond, the operating current will be 20 mA maximum rather than the 35 mA for 375 ns cycle time. Conversely it may be possible for some ITT 4116 to operate with shorter cycle times than 375 ns, provided all AC requirements are met; however, the increased power dissipation will require a reduction in ambient temperature.

Minimum overall system power requirements are achieved if $\overline{RAS}$ as opposed to $\overline{CAS}$ is used to chip select as unselected devices then are in low power (standby) mode regardless of $\overline{CAS}$.

Power Up

The ITT 4116 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to ensure compliance with the Absolute Maximum Ratings, ITT recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and Data Out to the inactive state.

After power is applied to the device, the ITT 4116 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

1024-Bit (256 x 4) Static CMOS RAM

Features

- 256 words x 4 bits
- Single power supply (+3 V)
- Static operation – no refreshing and clocks
- Three-state output
- Low voltage (+2 V) standby operation
- Low power consumption
- Specially developed as an external RAM for ITT's one chip CMOS processed microcomputer SAA6000

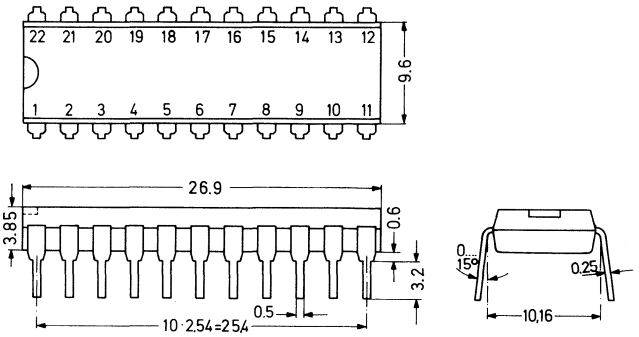


Fig. 2: ITT5101S in 22-Pin Plastic Package

Weight approximately 2 g
Dimensions in mm

General

The ITT5101S is a metal gate CMOS RAM with a capacity of 1024 bits (256 words x 4 bits). It uses only static (D.C.) circuitry and therefore requires no clocks. The memory has separate data input and output terminals. An output disable function is provided so that data inputs and outputs can be tied to a common data I/O system. Supply voltage is 2.6 to 3.2 V. Data retention is guaranteed at a supply voltage as low as 2.0 V.

Pin Connections

1	Address input A3	12	Data output DO2
2	Address input A2	13	Data input DI3
3	Address input A1	14	Data output DO3
4	Address input A0	15	Data input DI4
5	Address input A5	16	Data output DO4
6	Address input A6	17	Chip enable 2 CE2
7	Address input A7	18	Output disable OD
8	GND, 0	19	Chip enable 1 CE1
9	Data input DI1	20	Read/Write input R/W
10	Data output DO1	21	Address input A4
11	Data Input DI2	22	Supply Voltage V_{CC}

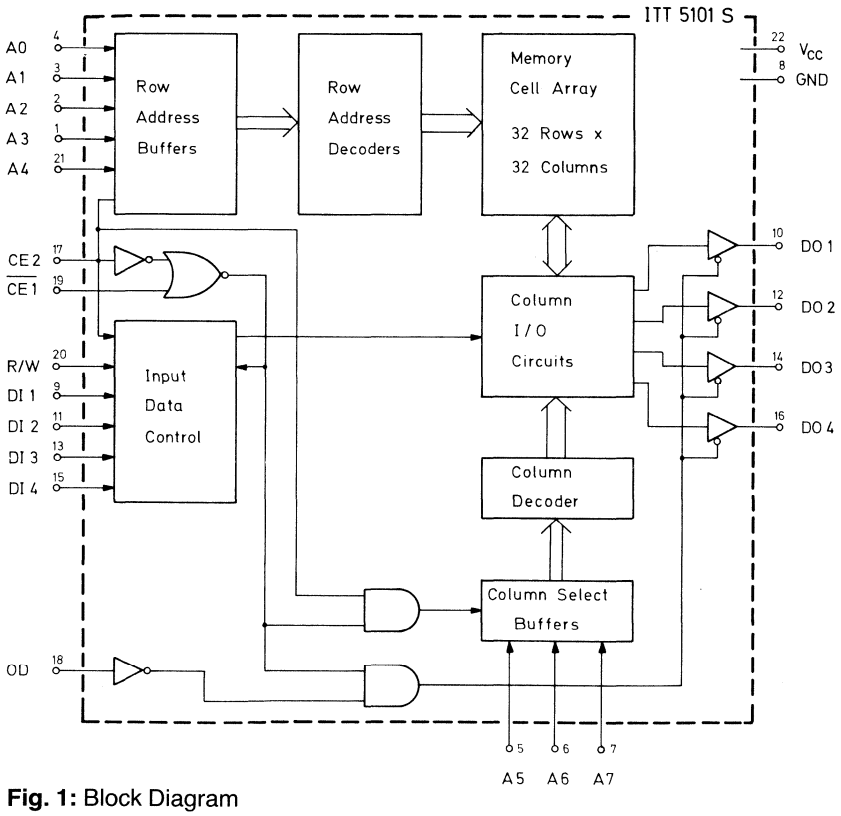


Fig. 1: Block Diagram

Table 1: Operation Modes

CE1	CE2	OD	R/W	D_{IN}	Output	Mode
H	X	X	X	X	High Z	Not Selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	D_{IN}	Write
L	H	L	H	X	D_{OUT}	Read

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC} [1)]	−0.3 to + 5.0	V
Input Voltage	V_I [1)]	−0.3 to V_{CC} + 0.3	V
Output Voltage	V_O [1)]	−0.3 to V_{CC} + 0.3	V
Ambient Operating Temperature Range	T_A	−5 to + 70	°C
Storage Temperature Range	T_S	−40 to +125	°C

[1)] Maximum voltage on any pin with respect to ground pin

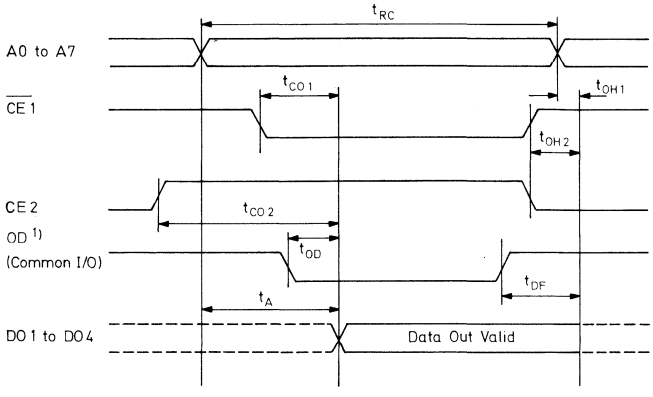


Fig. 3: Timing Diagram, Read Cycle
[1)] OD may be tied "Low" for separate I/O operation

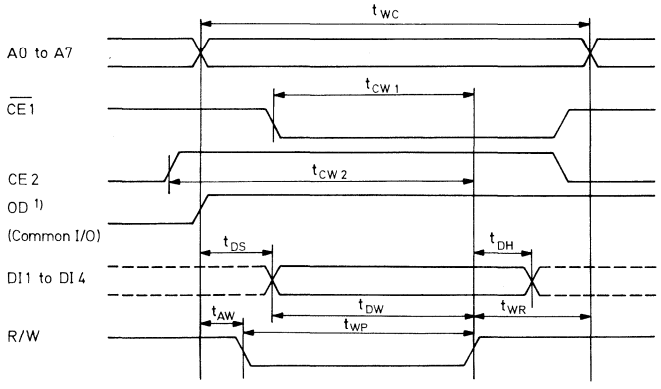


Fig. 4: Timing Diagram, Write Cycle
[1)] During the write cycle, OD is "High" for common I/O and "Don't Care" for separate I/O operation

DC Electrical Characteristics at $T_A = -5\,°C$ to $+70\,°C$, $V_{CC} = 2.6\,V$ to $3.2\,V$

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Low Voltage	V_{IL}	−0.3	–	0.6	V	
Input High Voltage	V_{IH}	1.8	–	V_{CC}	V	
Output Low Voltage	V_{OL}	–	–	0.3	V	$I_{OL} = 500\,\mu A$
Output High Voltage	V_{OH}	$V_{CC} - 0.6$	–	–	V	$-I_{OH} = 30\,\mu A$
Input Current	$\lvert I_{LI} \rvert$	–	–	1.0	µA	$V_I = 0\,V$ or $V_I = V_{CC}$
Output Leakage Current	$\lvert I_{LO} \rvert$	–	–	1.0	µA	$V_I = 0\,V$ or $V_I = V_{CC}$, $\overline{CE1} = 1.8\,V$
Operating Current	I_{CC1}	–	5	11	mA	$V_I = V_{CC}$, $\overline{CE1} \leq 0.6\,V$, Output open
	I_{CC2}	–	8	13	mA	$V_I = 2.2\,V$, $\overline{CE1} \leq 0.6\,V$, Output open
Standby Current	I_{CCL}	–	–	10	µA	$CE2 \leq 0.2\,V$

AC Electrical Characteristics at $T_A = -5\,°C$ to $+70\,°C$, $V_{CC} = 2.6\,V$ to $3.2\,V$
Read Cycle

Parameter	Symbol	Min.	Typ.	Max.	Unit
Read Cycle	t_{RC}	3.0	–	–	µs
Access Time	t_A	–	–	3.0	µs
Chip Enable (CE1) to Output	t_{CO1}	–	–	3.0	µs
Chip Enable (CE2) to Output	t_{CO2}	–	–	3.2	µs
Output Disable to Output	t_{OD}	–	–	1.3	µs
Data Output to High Z State	t_{DF}	0	–	750	ns
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0	–	–	ns
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0	–	–	ns

AC Electrical Characteristics at $T_A = -5\,°C$ to $+70\,°C$, $V_{CC} = 2.6\,V$ to $3.2\,V$
Write Cycle

Parameter	Symbol	Min.	Typ.	Max.	Unit
Write Cycle	t_{WC}	3.0	–	–	µs
Write Delay	t_{AW}	750	–	–	ns
Chip Enable ($\overline{CE1}$) to Write	t_{CW1}	2.2	–	–	µs
Chip Enable (CE2) to Write	t_{CW2}	2.2	–	–	µs
Data Setup	t_{DW}	1.5	–	–	µs
Data Hold	t_{DH}	370	–	–	ns
Write Pulse	t_{WP}	1.5	–	–	µs
Write Recovery	t_{WR}	180	–	–	ns
Output Disable Setup	t_{DS}	750	–	–	ns

AC Test Conditions

Input Pulse Levels	0.6 V to 1.8 V
Input Pulse Rise and Fall Times	20 ns
Timing Measurement Reference Level	1.1 V
Output Load	No Load

Capacitance at $T_A = 25\ °C$, $f = 1\ MHz$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance, $V_{IN} = 0\ V$	C_{IN}	–	6	10	pF
Output Capacitance, $V_{OUT} = 0\ V$	C_{OUT}	–	15	20	pF

Low V_{CC} Data Retention Characteristics at $T_A = 0\ °C$ to $70\ °C$[1)]

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{DR}	2.0	–	–	V	$V_{CE2} \leq 0.2\ V$
Data Retention Current	I_{CCDR}	–	–	20	µA	$V_{CE2} \leq 0.2\ V$, $V_{DR} = 2.0\ V$
Chip Deselect to Data Retention Time	t_{CDR}	0	–	–	ns	
Operation Recovery Time	t_R	t_{RC}[2)]	–	–	ns	

[1)] In Low V_{CC} data retention mode, all input and output voltages should be maintained under V_{DR}
[2)] t_{RC}: Read Cycle Time

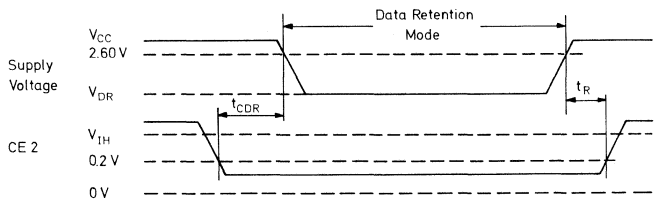


Fig. 5: Timing Diagram, Low V_{CC} Data Retention

ITT7163 – Quint Relay Driver

Features:

–65 V output rating, for –50 V battery operation

Operation also suitable for 24 V supplies

70 mA drive capability per element

Outputs can be paralleled for increased current capability

Non-destructive avalanche characteristics

Output protection against short circuits

TTL-compatible inputs

Input noise rejection

All inputs both current and voltage limited for complete protection

All DC supply connections are internally current-limited for the highest in-circuit reliability

Low junction temperature for the highest reliability

Internal input pull-up resistors

14-pin cerdip case or 14-pin plastic package TO-116

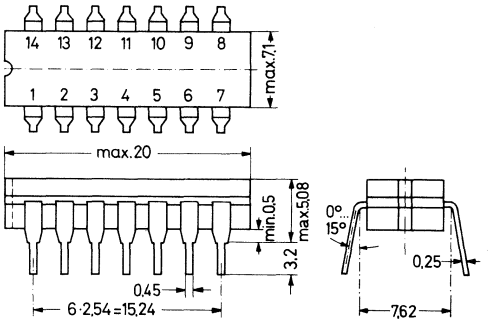


Fig 1:
ITT7163 in TO-116 Dil Cerdip Case, 20 A 14 according to DIN41866

Weight approximately 2 g
Dimensions in mm

General description

The ITT7163 is a monolithic relay driver circuit using Si-gate P-channel MOS technology. It is designed as an interface between relays powered by a –50 V (nominal) battery and TTL or DTL logic circuits. In terms of logic, each element is a voltage inverter. When any input is grounded, the corresponding output turns ON and the relay is activated. The relays turn off if the appropriate input is taken more positive than 2 V.

Each output in the ON state may be considered as a resistor of 25 Ω max. at a load current of 40 mA, the maximum permissible continuous load current being 70 mA. The outputs of any one package may be connected in parallel to provide larger currents and/or lower output voltages. With all five outputs in parallel the device is equivalent to a 5 Ω resistor with a load of 250 mA.

A special feature of the ITT7163 is that the ground of the electronic logic (input ground, "quiet ground") and the ground line for the relays (output ground, "noisy ground") do not have to be at the same voltage. The ITT7163 is, therefore, suitable for use in physically large equipments, such as telephone exchanges, where significant voltage differences can exist in practice between ground lines that are connected together and should be at the same potential.

In addition to the normal noise margin obtainable when the circuit is driven by TTL, the ITT7163 contains delay circuits which reject input noise transients lasting up to (typically) 50 μs.

With an inductive load it is recommended that a diode be used to clamp the backswing of the load, without a diode the ITT7163 output stage may avalanche.

The input threshold of the ITT7163 is compatible with all TTL circuits as only a very small input current of about 15 μA is required. Each input is protected against static charge with the conventional gated diode voltage limiting circuit. In addition, there is an internal polysilicon resistor in series with each input. This 10 kΩ resistor limits the current that can flow into the drive circuit in the event of the ITT7163 being misused so that a low impedance path exists between the relay supply voltage and the substrate of the ITT7163.

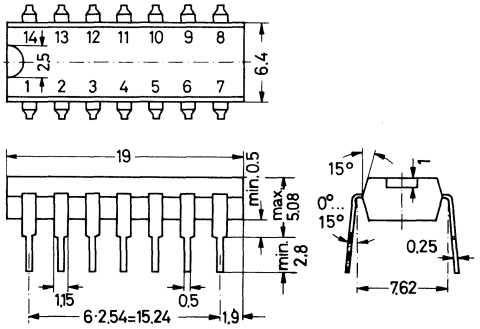


Fig. 2:
ITT7163 in TO-116 Dil Plastic Package, 20 A 14 according to DIN 41866

Weight approximately 1.2 g
Dimensions in mm

Pin Connections

1	Supply voltage V_{GG}	8	Noisy ground NG
2	Output of driver 1	9	Input of driver 5
3	Output of driver 2	10	Input of driver 4
4	Output of driver 3	11	Input of driver 3
5	Output of driver 4	12	Input of driver 2
6	Output of driver 5	13	Input of driver 1
7	Electronic ground EG	14	Supply voltage V_{CC}

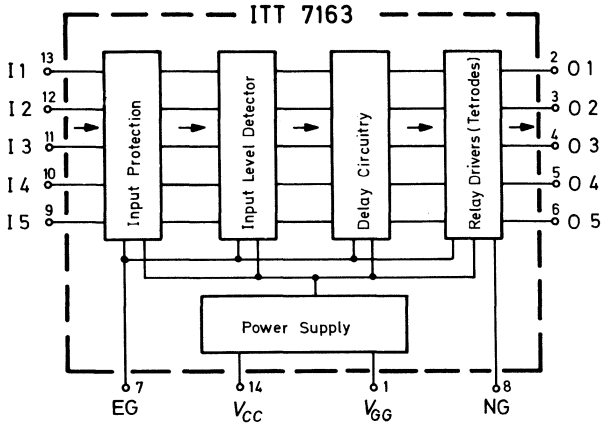


Fig. 3: ITT7163 Block diagram

Absolute Maximum Ratings

	Symbol	Value	Unit	Conditions
Power Dissipation at T_A = 70 °C	$P_{tot\,1}$	700	mW	$T_{j\,max}$ = 125 °C
	$P_{tot\,2}$	255	mW	$T_{j\,max}$ = 90 °C
Storage Temperature Range	T_S	–65 to +150	°C	
Input Voltage Range, referred to Pin 14	V_I	–60 to +3	V	
Negative Output Voltage, referred to Pin 8 (NG)				
continuous	V_O	–65	V	
Transient from a 500 Ω Source	V_{OT}	–75	V	Note 1
Negative Supply Voltage, referred to Pin 8 (NG)	V_{GG}	–33	V	
Positive Supply Voltage Range, referred to Pin 7 (EG)	V_{CC}	–0.3 to +20	V	
Voltage Range of Pin 8 (NG),				
referred to Pin 7 (EG)	V_{NG}	–5.25 to +5.25	V	
referred to Pin 14 (V_{CC})	V_{NG}	–20 to +1	V	
Continuous Output Current (Each Element), all Drivers operating	I_O	–70	mA	

Note 1: This rating applies for a 20 ms single surge and V_{GG} over the full operating range. Also a voltage variation of up to ±30 V can be applied between electronic ground and noisy ground simultaneous with the increase in voltage on all outputs up to 75 V.

Recommended Operating Conditions

	Symbol	Min.	Typ.	Max.	Unit	Conditions
Ambient Temperature	T_A	0	–	70	°C	Note 2
Supply Voltages	V_{CC}	4.75	5	5.25	V	
	$-V_{GG}$	23.5	27	32	V	
Input Voltages						
for Output OFF state	V_{IH}		2.0 V to V_{CC} +0.3 V		–	
for Output ON state	V_{IL}	0	–	0.8	V	
Noisy Ground Voltage	V_{NG}	–4	–	+4	V	
Continuous Output ON Current	I_{OH}	–	–	–70	mA	Fig. 4

Note 2: Operation below 0 °C is permissible providing the increase in I_{GG} can be accomodated in the bias circuit.

D. C. Characteristics and Operating Conditions

Output voltage and battery voltage are referred to pin 8. All other voltages are referred to pin 7. $V_{7/8} = 0$ V.

Characteristics, over full range of recommended operating conditions except where stated.

	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output OFF state Current	$-I_L$	–	–	50	μA	$-V_{OL} = 60$ V, $-V_{GG} = 32$ V see also Note 3, $V_{7/8} = 0$ V
Output Breakdown Voltage	$-V_{O1}$	65	–	–	V	$-I_{OL} = 1$ mA, $V_{7/8} = 0$ V, $-V_{GG} = 32$ V
	$-V_{O2}$	60	–	–	V	$-I_{OL} = 1$ mA, $V_{7/8} = 0$ V, $-V_{GG} = 27$ V
	$-V_{O3}$	56	–	–	V	$-I_{OL} = 1$ mA, $V_{7/8} = 0$ V, $-V_{GG} = 23$ V
Output ON state Resistance	R_{OH}	–	–	25	Ω	$-I_{OH} = 40$ mA (see Fig. 6)
Output ON state Voltage (each output)	$-V_{OH}$	–	–	1	V	$-I_{OH} = 40$ mA
Output ON state Voltage (Note 4)	$-V_{OH}$	–	–	1.25	V	$-I_{OH} = 250$ mA (total package)
Input Current						
High-state	$-I_{IH}$	2	–	22	μA	$V_{IH} = 2$ V
Low-state	$-I_{IL}$	2	–	25	μA	$V_{IL} = 0.8$ V
Internal Temperature Rise all Outputs ON	T_j-T_A	–	–	20	°C	$-I_O = 40$ mA (Note 5)
Current Consumption						
	I_{CC}	–	–	2.5	mA	$V_{CC} = 5.25$ V
	$-I_{GG}$	0.5	–	1.3	mA	$-V_{GG} = 27$ V, $T_A = 25$ °C
	$-I_{GG}$	0.31	–	2	mA	$-V_{GG} = 23.5$ to 32 V, $T_A = 0$ to 70 °C
	$-I_{GG}$	0.53	–	1.4	mA	$-V_{GG} = 32$ V, $T_A = 70$ °C
	$-I_{GG}$	–	–	1.15	mA	$-V_{GG} = 23.5$ V, $T_A = 0$ °C

Note 3: The following two sets of conditions also apply: 1) $-V_{OL} = 55$ V, $-V_{GG} = 27$ V 2) $-V_{OL} = 51$ V, $-V_{GG} = 23$ V
Note 4: All outputs and inputs connected in parallel
Note 5: Measured with the ITT7163 package soldered into a p.c. board

A. C. Characteristics

	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Capacitance	C_I	–	–	5	pF	
Propagation Delay Time	t_{pd}	1	50	300	μs	Fig. 4

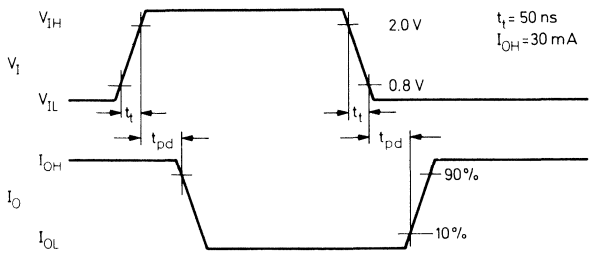


Fig. 4: Timing diagram

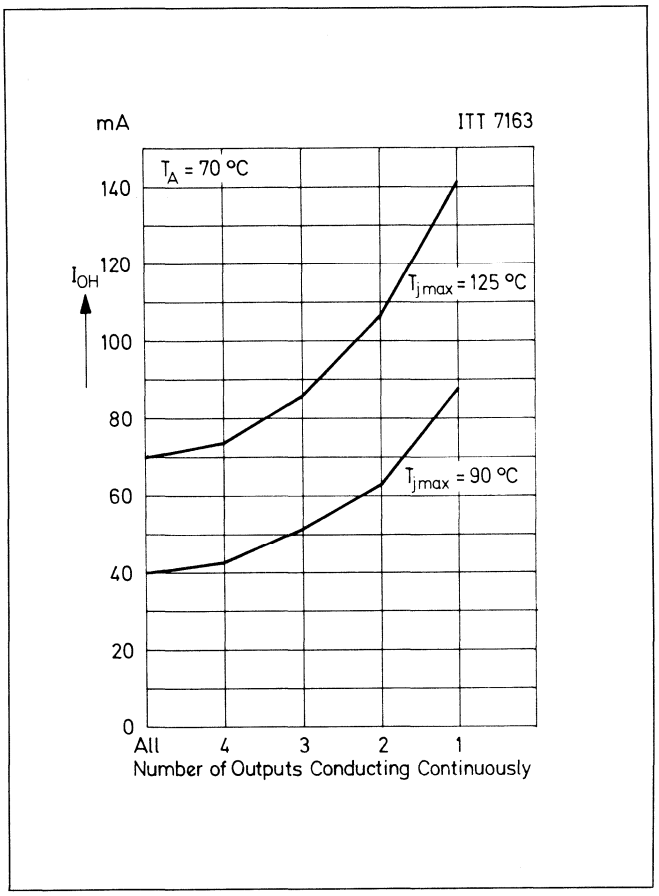


Fig 5: Variation of the maximum current rating per output depending on the number of outputs continuously conducting. This is important in some systems such as control and coded signals where not all outputs are conducting continuously.

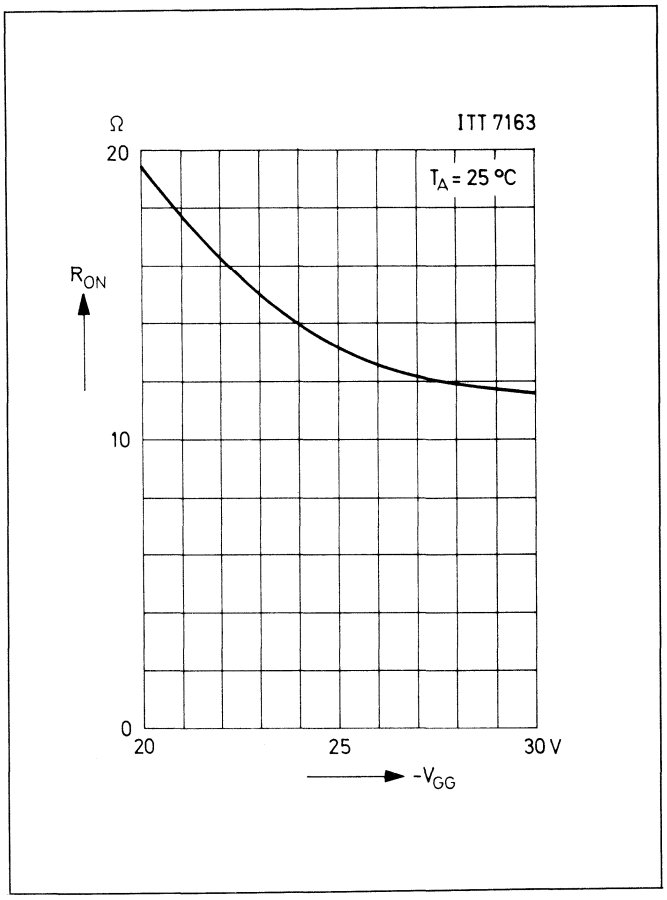


Fig. 6: Equivalent ON state resistance versus V_{GG} supply voltage. This is approximately independent of the load current up to 70 mA.

Circuit Function under Fault Conditions

Should the relay quench diode fail and short the battery supply to one of the output pins, catastrophic failure will not occur. The output transistor will be biased into the saturated, or "constant-current", state thus limiting the current passed to ground. The resulting high dissipation will increase the chip temperature, thus further reducing the current to, typically, 60 mA.

Applications Information

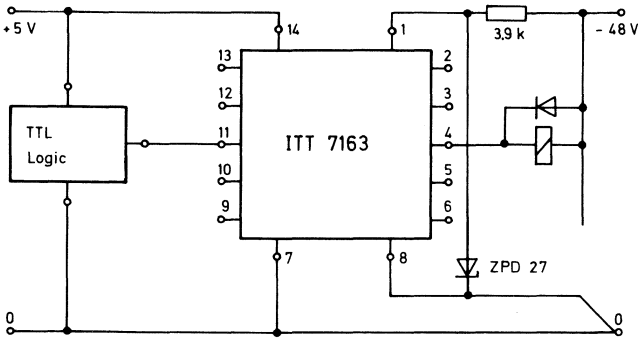


Fig. 7: Typical application circuit

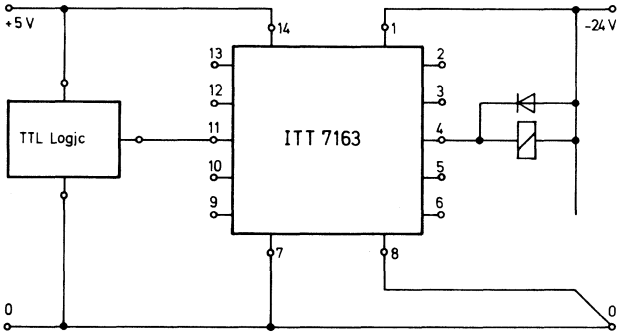


Fig. 9: ITT 7163 application circuit for 24 V supply voltage

If the loads are connected to the ITT 7163 via a long multicore cable then care must be taken to ensure that switching transients greater than 75 V do not appear between the negative side of the battery and noisy ground. Open circuit or ground conditions may be applied to the outputs subject to the above limitation.

The circuit shown in Fig. 8a is designed to supply one ITT 7163 package. The bias circuits Fig. 8b and c can feed several packages ITT 7163, and the maximum number is dependent upon the permitted maximum dissipation of the transistor. With no restriction on dissipation the fanout would be at least 20 but, with maximum junction temperatures restricted to 125 °C the fanout is restricted to a maximum of 12. The fanout must be further reduced for lower maximum temperatures. Under these conditions the current-limiting resistor in series with the collector can be increased. The 1% resistors are assumed to have an end of life tolerance of ±3%. It is also assumed that the voltage between the negative end of the battery and noisy ground is kept within the limits –44.5 V to –52 V. The main advantage of the bias circuits containing resistive divider networks, Fig. 8a and c, is that there is a reasonable degree of tracking between the value of V_{GG} and the value of voltage applied to the outputs (battery voltage in the relay OFF condition). Since the breakdown voltage of ITT 7163 increases with increasing V_{GG} (and battery voltage), the circuit allows a high safety margin between battery voltage (OFF state voltage applied to the outputs) and breakdown voltage of the outputs.

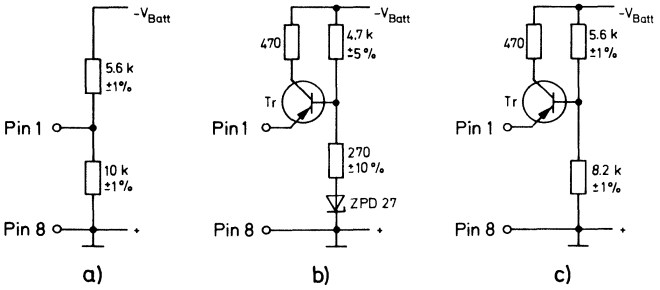


Fig. 8: Variety of bias networks which can provide the DC supply V_{GG} at pin 1 for the ITT 7163, alternative to the solution shown in Fig. 7. The transistor Tr is a 2N2905A type with heat sink clip of 50 °C/W.

The ITT 7163 can be used as a relay driver for relays which operate on a nominal 24 V positive ground supply. Its current capability means that relay coils can be switched which operate with a nominal power of 1 W. The appropriate application circuit is shown in Fig. 9.

ITT7164 – Quint Relay Driver with Integrated Temperature Sensing Diode

Features:
Integrated diode to sense a short-circuit load
All electric characteristics the same as the ITT7163
16-pin cerdip case or 16-pin plastic package

General Description

The ITT7164 is identical electrically to the ITT7163 quint relay driver except the ITT7164 includes a sensing diode to indicate any excessive load condition such as a short circuit relay coil or its quench diode if included.

The forward voltage drop of sensing diode FD is compared with the base emitter voltage of a transistor connected externally. If the forward voltage drop of the diode decreases due to overheating, the transistor will produce a signal which may be used with an indicator or may turn off the device with failure condition. The sensing diodes of up to ten ITT7164 circuits can be paralleled to drive a common sensing amplifier.

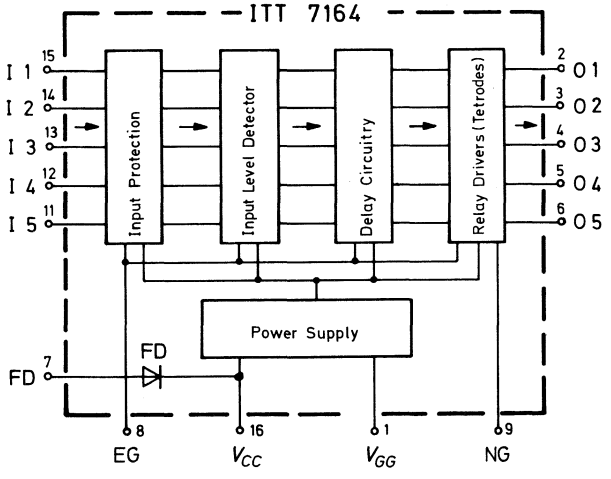


Fig. 10: ITT7164 Block diagram

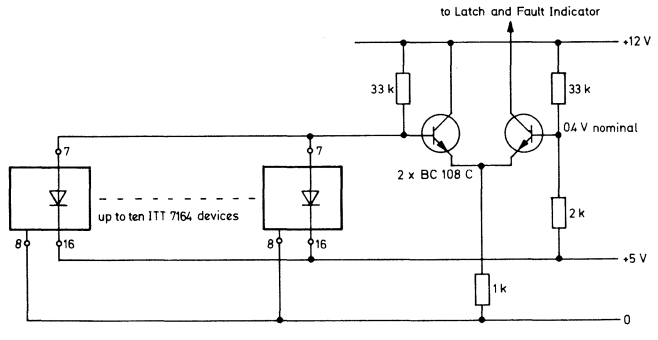


Fig. 13: Proposed circuit diagram for the sensing amplifier

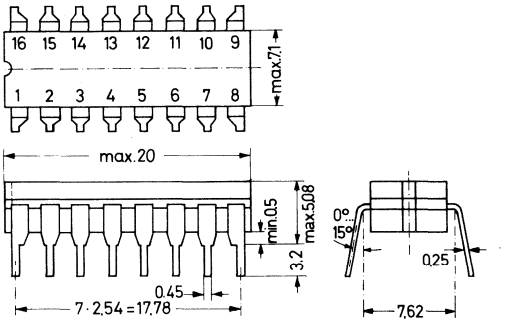


Fig. 11:
ITT7164 in 16-pin Dil
Cerdip case, 20 A 16
according to DIN 4 1866

Weight approximately 2 g
Dimensions in mm

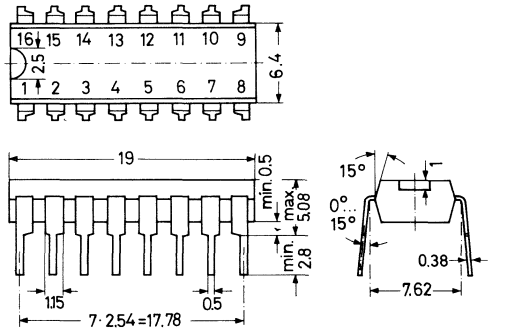


Fig. 12:
ITT7164 in 16-pin Dil
Plastic package, 20 A 16
according to DIN 41866

Weight approximately 1.2 g
Dimensions in mm

Pin Connections

1	Supply voltage V_{GG}	9	Noisy ground NG
2	Output of driver 1	10	NC
3	Output of driver 2	11	Input of driver 5
4	Output of driver 3	12	Input of driver 4
5	Output of driver 4	13	Input of driver 3
6	Output of driver 5	14	Input of driver 2
7	Anode of sensing diode	15	Input of driver 1
8	Electronic ground EG	16	Supply voltage V_{CC}

Characteristics of the Sensing Diode

Forward Voltage Drop at I_{ON} = 20 μA, operation with normal load	$V_{ON\,1}$	0.55 to 4	V
at I_{ON}= 300 μA, with output(s) turned ON and connected directly to –50 V (short directly circuit load(s))	$V_{ON\,2}$	<0.25	V

1. Introduction

Designed in low-threshold CMOS technology, the SAA6000 has a 3 V supply voltage and an extremely low current consumption of 15 to 45 μA depending on the mode of operation.

The SAA6000 contains on a single silicon chip of a few square millimeters area a 2268 byte ROM, a RAM of 96 words, 8 static shift registers with 9 bits each, a 15-stage frequency divider, the clock oscillator, ALU and accumulator, programmable logic arrays (PLA), and other logic circuits; see Fig.2. Due to its extremely flat construction – 2 mm in height – the SAA6000 is suited for application in equipment no thicker than a pocket notebook. Some of the typical application examples are:

– programmable IR transmitters for cordless remote control
– auto dialler for intelligent pushbutton telephone subsets
– taximeters
– clock calculators
– precision clocks
– stop watches
– cash registers
– vending machines
– controllers for various home electric appliances
– heart-rate monitors
– drivers for LCDs
– hand-held instruments (thermometers etc.)
– controllers for toys and games

In addition, upon the customer's request, many other applications are available.

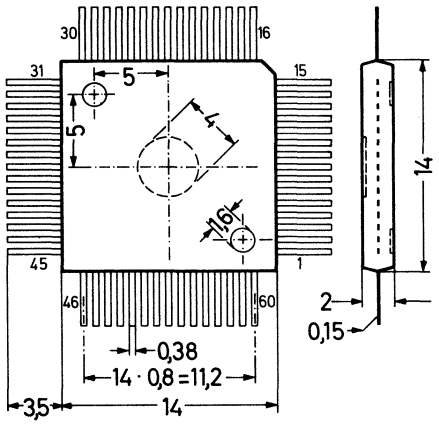


Fig.1: SAA6000 in plastic package
Weight approx. 0.8g
Dimensions in mm

Features:

– Complete one-chip microcomputer
– ROM capacity : 2268 bytes
– RAM capacity : 96 words of 4 bits each
– Instruction set : 54 instructions
– Subroutine level : 1 level
– Input port K input : 4 bits
– Asynchronous input : 2 bits
– Output port O_{ij} : 34 bits
H_i : 3 bits
R_i : 4 bits
– Input/output port DIO : 4 bits
– Divider of 15 stages with reset
– Internal LCD drive circuit
– External RAM drive
– Internal crystal oscillator circuit
– Extremely small power consumption
– Internal low-voltage detection circuit
– 60 pin quad package

2. Block Diagram

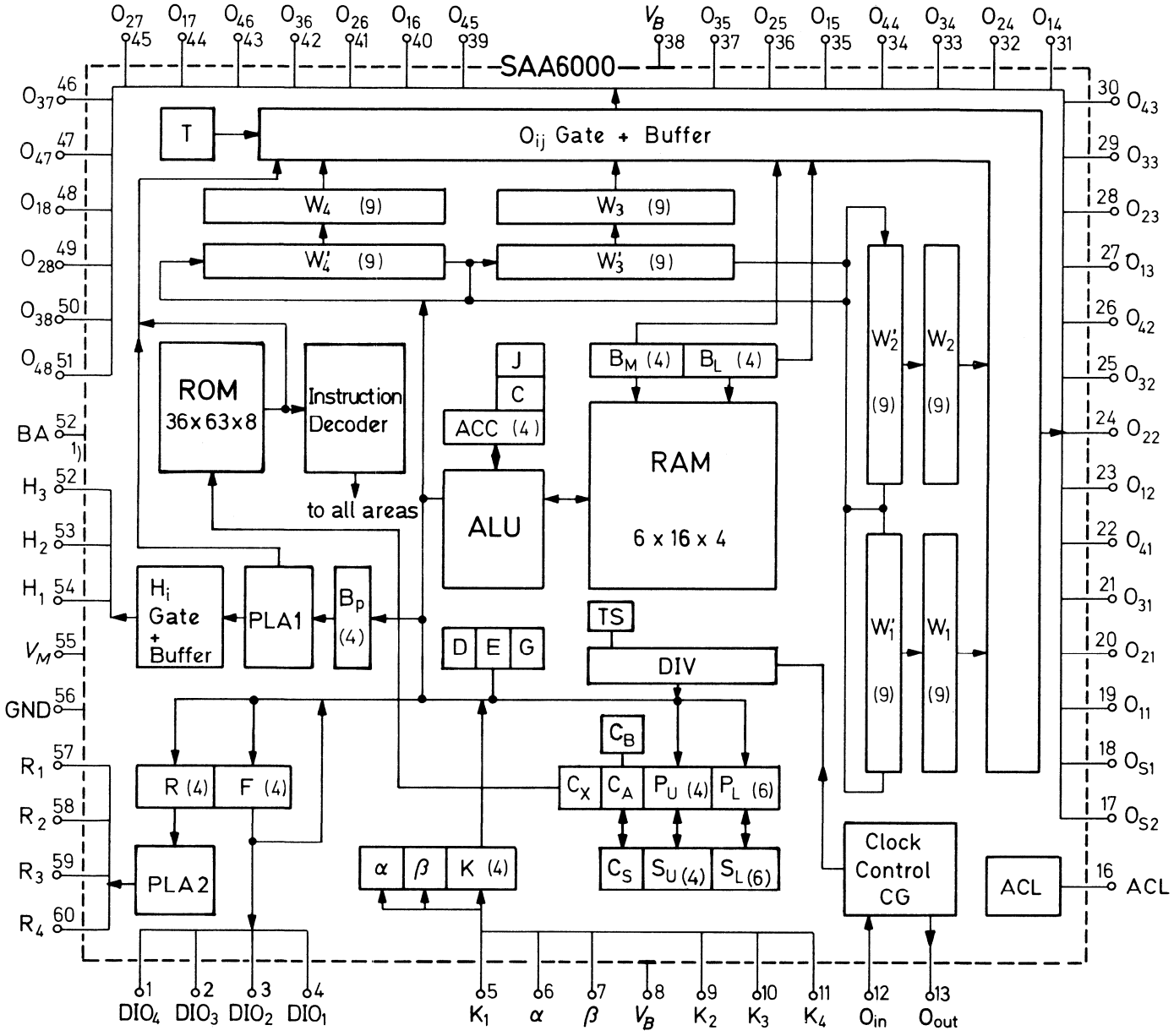


Fig. 2: Block diagram of the one-chip microcomputer SAA 6000

Pin Connections

$O_{11}...O_{48}$, O_{S1}, O_{S2}	Outputs
H_1 to H_3 [1])	Outputs, three-level
R_1 to R_4	Outputs
DIO_1 to DIO_4	Inputs/Outputs, tri-state
α and β	Asynchronous inputs
K_1 to K_4	Inputs
BA [1])	Input for low-voltage detection
O_{in}, O_{out}	Crystal oscillator terminals
GND	Ground, negative potential of supply voltage
V_B	Positive potential of supply voltage
V_M	Center tap of supply voltage
ACL	Switch-on initialisation

[1]) Because the number of terminals on the package is limited, either BA or H_3 is to be selected.

3. Electrical Parameters

All voltages are referred to ground (GND).

Absolute Maximum Ratings

	Symbol	Value	Unit
Supply Voltages	V_B	−0.3 to +3.5	V
	V_M	−0.3 to +3.5	V
Ambient Operating Temperature Range	T_{amb}	−5 to +55	°C
Storage Temperature Range	T_S	−20 to +70	°C

Recommended Operating Conditions

	Symbol	Min.	Typ.	Max.	Unit
Supply Voltages	V_B	+2.6	–	+3.4	V
	V_M	0.45 V_B	0.5 V_B	0.55 V_B	V
Oscillator Frequency	f_{osc}		32768		Hz

Characteristics at V_B = +2.9 to +3.2 V, T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Current Consumption					
Standby Mode with LCD Clock Drive	$+I_D$	–	15	25	μA
in full Operation	$+I_D$	–	45	60	μA
Input Currents, Inputs ACL, α, β, DIO					
Low State (logic 0)	$-I_{IL}$	–	–	15	μA
High State (logic 1)	I_{HL}	–	–	15	μA
Input Voltages, Inputs K_1 to K_4, α, β					
Low State (logic 0)	V_{IL}	0	–	+0.6	V
High State (logic 1)	V_{IH}	V_B −0.6	–	V_B	V
Input Voltage, Input ACL					
Low State (logic 0)	V_{IL}	0	–	+0.3	V
High State (logic 1)	V_{IH}	V_B −0.3	–	V_B	V
Output Current, Outputs O_{11} to O_{48}, O_{S1}, O_{S2}, DIO_1 to DIO_4, R_2 to R_4	I_O	–	50	–	μA
Output R_1	I_O	–	100	–	μA
Voltage Drop Across the Output Transistors, Outputs O_{11} to O_{48}, O_{S1}, O_{S2}, DIO_1 to DIO_4, R_2 to R_4 at I_O = 50 μA	ΔV	–	–	0.5	V
Output R_1 at I_O = 100 μA	ΔV	–	–	0.2	V
Instruction Cycle for 1 byte Instructions	t_{i1b}	–	$\frac{2}{f_{osc}}$	–	s
Instruction Cycle for 2 byte Instructions	t_{i2b}	–	$\frac{4}{f_{osc}}$	–	s

4. Explanation of Functions

4.1. Brief Description

In order to make the most efficient use of the available silicon area, the architecture of the SAA6000 includes not only conventional building blocks, such as program memory, RAM, ALU and accumulator, but also a variety of more or less special-purpose elements associated with certain inputs and outputs.

The program counter C_X, C_A, P_U, P_L addresses the instructions in the ROM. Instructions are processed by the instruction decoder, which controls all movement and processing of data. One subroutine level is provided for by the stack registers C_S, S_U, S_L.

Working data stored in the RAM is addressed by the B_M, B_L registers. Data processing is performed by the ALU, with the accumulator and the C flip-flop as destination. Instructions provide for four-bit parallel data transfer from the accumulator to the B_p, F and R registers and to the first bits of the W' registers. 4-bit words can also be stored in the RAM, or individual bits in the RAM can be set or reset.

The B_p registers feed the H_i and O_{ij} outputs via PLA1, which allows the generation of various kinds of strobe signals, e.g. as backplate drive signals for LCDs. The R_i outputs can be treated as a general-purpose output port, but by the use of the associated PLA2 they can be turned into individual strobes, e.g. for controlling data transfers via the DIO port. The DIO port is a general purpose I/O port, especially suited for access to external RAM(s). The W' registers are used to assemble data in serial form for parallel transfer to the W registers or to the O_{ij} outputs. Some of the O_{ij} outputs are provided with data highways from the ROM outputs or the RAM address registers B_M and B_L as well as from the W' and W registers. Thus, in addition to their normal function of displaying data, they can address external RAM and display the contents of the ROM.

Apart from the DIO port, the main input port is the four-bit K port, typically used for keyboard scanning, the scanning strobes being supplied by as many O_{ij} outputs as necessary. The α and β inputs are single inputs, typically used for testing external conditions. The BA input is, like the α and β inputs, associated with an individual test instruction and may be used similarly as a logic input, but its main purpose is to detect low supply voltage.

The internal divider driven by a clock generator can be read and reset by software. Its final (1 s) output sets the TS flip-flop, which is testable by an instruction, so that time-of-day functions are easily implemented.

4.2. Accumulator ACC and Arithmetic Logic Unit ALU

The accumulator is a 4-bit working register. It holds operands and results of computations of the ALU. It also executes the data exchange between the RAM and the input and output ports. The ALU has a capacity of 4 bits and performs arithmetic, logic and transfer operations. Decimal addition and subtraction can be carried out by appropriate instructions or combinations of instructions.

4.3. ROM (Program Memory) and Program Counter

The ROM has a capacity of 2268 bytes, and consists of 36 pages × 63 instructions (steps), each having 8 bits. The program counter consists of 1-bit registers C_X and C_A, 4-bit register P_U and 6-bit polynomial counter P_L.

The 36 pages are divided into two fields of 16 pages each and one field of 4 pages (Fig. 3). The steps are defined by polynomial counter P_L, pages by register P_U, and fields by registers C_X and C_A. $C_X = 1$ defines the subroutine field.

	C_X	0		1
P_U	C_A	0	1	*
0		00	10	S0
1		01	11	S1
2		02	12	S2
3		03	13	S3
4		04	14	
5		05	15	
6		06	16	
7		07	17	
8		08	18	
9		09	19	
A		0A	1A	
B		0B	1B	
C		0C	1C	
D		0D	1D	
E		0E	1E	
F		0F	1F	

Fig. 3:
Page and field configuration of the ROM (* = redundant code)

When switching on the power supply, the address starts from (C_X, C_A, P_U, P_L) = 0, 0, F, 0, hexadecimal addressing. This requires a capacitance between terminal ACL and V_B. The ACL input must be held at the H level for a minimum of 6 oscillator cycles, i.e. 183 μs min. The capacitance value required to achieve this depends on the rise-time of the supply voltage, but a typical value is 470 nF. The first instruction byte at address 0, 0, F, 0 must be a dummy instruction, because it is not executed. Except in the case of jump instructions, the polynomial counter P_L is normally incremented step by step according to the polynomial code (see Fig. 4). At the end of a page P_L is incremented in the usual way, but there is no automatic change of page: to change pages a jump instruction is required.

TR0, TR1, SSR, COMCB, RTN0, RTN1 and JMP belong to the group of jump instructions, and by the combination of these instructions, Page, Field and Subroutine jumps are performed. A detailed description of the jumps will be given later (see section 5.3.).

The stack consists of registers C_S of 1 bit, S_U of 4 bits, and S_L of 6 bits. One level of subroutine nesting can be performed.

Step	Polynomial counter P_{L6} P_{L5}	P_{L4} P_{L3} P_{L2} P_{L1}	Hex code	Step	Polynomial counter P_{L6} P_{L5}	P_{L4} P_{L3} P_{L2} P_{L1}	Hex code	Step	Polynomial counter P_{L6} P_{L5}	P_{L4} P_{L3} P_{L2} P_{L1}	Hex code
1	0 0	0 0 0 0	00	22	0 1	1 0 1 0	1A	43	1 0	0 1 0 1	25
2	1 0	0 0 0 0	20	23	0 0	1 1 0 1	0D	44	0 1	0 0 1 0	12
3	1 1	0 0 0 0	30	24	0 0	0 1 1 0	06	45	0 0	1 0 0 1	09
4	1 1	1 0 0 0	38	25	0 0	0 0 1 1	03	46	0 0	0 1 0 0	04
5	1 1	1 1 0 0	3C	26	1 0	0 0 0 1	21	47	1 0	0 0 1 0	22
6	1 1	1 1 1 0	3E	27	0 1	0 0 0 0	10	48	0 1	0 0 0 1	11
7	0 1	1 1 1 1	1F	28	1 0	1 0 0 0	28	49	0 0	1 0 0 0	08
8	1 0	1 1 1 1	2F	29	1 1	0 1 0 0	34	50	1 0	0 1 0 0	24
9	1 1	0 1 1 1	37	30	1 1	1 0 1 0	3A	51	1 1	0 0 1 0	32
10	1 1	1 0 1 1	3B	31	0 1	1 1 0 1	1D	52	0 1	1 0 0 1	19
11	1 1	1 1 0 1	3D	32	0 0	1 1 1 0	0E	53	0 0	1 1 0 0	0C
12	0 1	1 1 1 0	1E	33	0 0	0 1 1 1	07	54	1 0	0 1 1 0	26
13	0 0	1 1 1 1	0F	34	1 0	0 0 1 1	23	55	0 1	0 0 1 1	13
14	1 0	0 1 1 1	27	35	1 1	0 0 0 1	31	56	1 0	1 0 0 1	29
15	1 1	0 0 1 1	33	36	0 1	1 0 0 0	18	57	0 1	0 1 0 0	14
16	1 1	1 0 0 1	39	37	1 0	1 1 0 0	2C	58	1 0	1 0 1 0	2A
17	0 1	1 1 0 0	1C	38	1 1	0 1 1 0	36	59	0 1	0 1 0 1	15
18	1 0	1 1 1 0	2E	39	0 1	1 0 1 1	1B	60	0 0	1 0 1 0	0A
19	0 1	0 1 1 1	17	40	1 0	1 1 0 1	2D	61	0 0	0 1 0 1	05
20	1 0	1 0 1 1	2B	41	0 1	0 1 1 0	16	62	0 0	0 0 1 0	02
21	1 1	0 1 0 1	35	42	0 0	1 0 1 1	0B	63	0 0	0 0 0 1	01

Fig. 4: Polynomial code for the program counter P_L

B_L	file	X	Y	Z	M	U	T
	B_{M3}	0	0	0	0	1	1
	B_{M2}	0	0	1	1	*	*
	B_{M1}	0	1	0	1	0	1
0		00	10	20	30	40	50
1		01	11	21	31	41	51
2		02	12	22	32	42	52
3		03	13	23	33	43	53
4		04	14	24	34	44	54
5		05	15	25	35	45	55
6		06	16	26	36	46	56
7		07	17	27	37	47	57
8		08	18	28	38	48	58
9		09	19	29	39	49	59
A		0A	1A	2A	3A	4A	5A
B		0B	1B	2B	3B	4B	5B
C		0C	1C	2C	3C	4C	5C
D		0D	1D	2D	3D	4D	5D
E		0E	1E	2E	3E	4E	5E
F		0F	1F	2F	3F	4F	5F

Fig. 5: Organization of the internal RAM
(* = redundant code)

4.4. RAM (Data Memory)

The capacity of the RAM is 384 bits, organized as 6 × 16 words of 4 bits each. The RAM is addressed by registers B_L and B_M (4 bits each) – see Fig. 5. B_{M4} is used only when addressing external RAM: it is redundant when addressing internal RAM.

4.5. Inputs

4.5.1. K_i Input Port (i = 1 to 4)

K_i is a 4-bit input port. The logic levels on the K_i inputs can be loaded into the accumulator by the KTA instruction. All K_i inputs have internal pull-down resistors. The value of the pull-down resistors on the K_i inputs is typically 100 KΩ, with limits of 50 K...200 KΩ.

4.5.2. Asynchronous Inputs α and β

The inputs α and β can be tested independently by the TA and the TB instructions respectively. The α flip-flop is set by the L → H edge of the α input and reset by the TA instruction. If an input signal (i.e. a H level) arrives at the α input while the TA instruction is being executed, it is correctly accepted either at the time or on the next occasion that the TA is executed. It is not possible for an input signal to be missed by reason of the time of its arrival. The β flip-flop is a D-type flip-flop which is triggered by the internal clock, its D input being connected to the β input. The β input is therefore not reset by the TB instruction.

4.5.3. BA Terminal

The BA terminal may be used as a normal input, but it is also possible to use this terminal for detecting whether a voltage exceeds an upper or a lower limit. As shown in Fig. 6, there is a Schmitt-trigger and a pull-up resistor on the chip connected to this BA terminal. If, for example, an external resistor is connected between BA and GND, then the voltage supplied to the

Schmitt-trigger depends on the ratio of the two resistors and on the supply voltage. The TAL instruction tests the output of the Schmitt-trigger. If the output is logic 1 – supply voltage is normal – the instruction following the TAL instruction is skipped. If the supply voltage drops below the level to be detected, the Schmitt-trigger output becomes logic 0 and the instruction following the TAL instruction is executed. The pull-up device on the BA input is turned on by the TAL instruction, i.e. it is not in circuit continuously. The 250 KΩ typical resistance has limits of 125K...500KΩ.

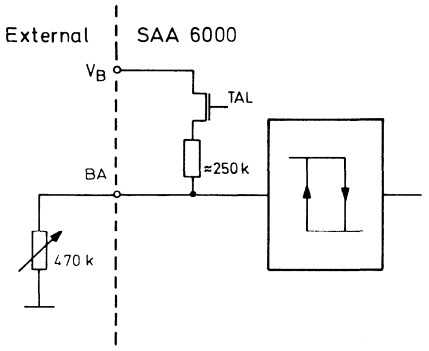


Fig. 6: Low voltage detection

4.6. Outputs and Programmable Logic Arrays (PLAs)

4.6.1. R_i Output Port (i = 1 to 4) and PLA2

The contents of the accumulator can be read out through the 4-bit output port R_i. However, this port may also be used to read out internal signals and logical combinations of them via PLA2.

The following signals are applied as inputs to PLA2:
R_1 to R_4 flip-flop outputs
$\overline{O_{S4}}$
$\overline{O_{S3}}$
f_i; $\overline{f_i} = f_1 \wedge f_4 \wedge f_{13}$. The signal f_i is programmable to a certain extent. The signal comes from the output of a three-input NAND gate. Any of the three inputs f_1, f_4 and f_{13} may be omitted, giving possibilities such as $f_i = \overline{f_4}$ or $f_i = \overline{f_1 \wedge f_{13}}$ etc. The pattern given by $f_i = \overline{f_1 \wedge f_4 \wedge f_{13}}$ is useful as an audible signal, e.g. for an alarm output.
$|\overline{\Phi_1}|$; $\overline{\Phi_1}$ is phase 1 of the system clock. The frequency is $\frac{1}{2} \cdot f_{osc}$. The mark-space ratio is about 1 : 2.
$\overline{I_1}$
I_1
$\overline{52}$; $\overline{52}$ is an internal signal, generated during the execution of the READ or WRITE instruction, and is at low level for the time $t_{i1b} = \frac{2}{f_{osc}}$.

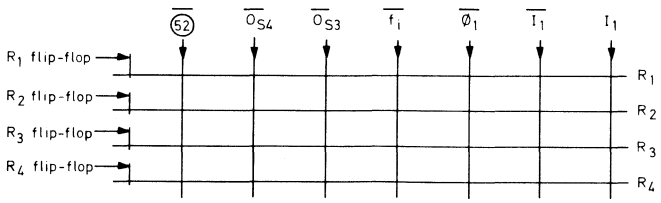


Fig. 7: Matrix construction of PLA2

Fig. 7 shows the matrix construction of PLA2. The matrix can be constructed with AND or with OR combinations of the input signals. The exact logical function on each R output must be formulated by starting from the left-hand end of Fig. 7. Each node in Fig. 7 (i.e. the intersection of a horizontal line with a vertical line) may be implemented as a 2-input-AND or -OR function with one input coming from the vertical line and the other input from the signal or logic function present to the left of the node. Example: If the R_1 line is programmed to give OR, AND, AND, OR, OR, AND, OR function starting from the left-hand end, the overall logic function is as follows:
$R_1 = ((((R_1 \text{ flip-flop} \vee \overline{52}) \wedge \overline{O_{S4}} \wedge \overline{O_{S3}}) \vee \overline{f_i} \vee \overline{\Phi_1}) \wedge \overline{I_1}) \vee I_1$
It is also possible to obtain O_{S3} and O_{S4} at the R outputs. In this case logical interconnection with other input signals is not allowed.

It is possible to add another logic function whereby the R_1 flip-flop is reset directly by a H level on the β input. If this function is not required, there is no connection between β and the R_1 flip-flop.

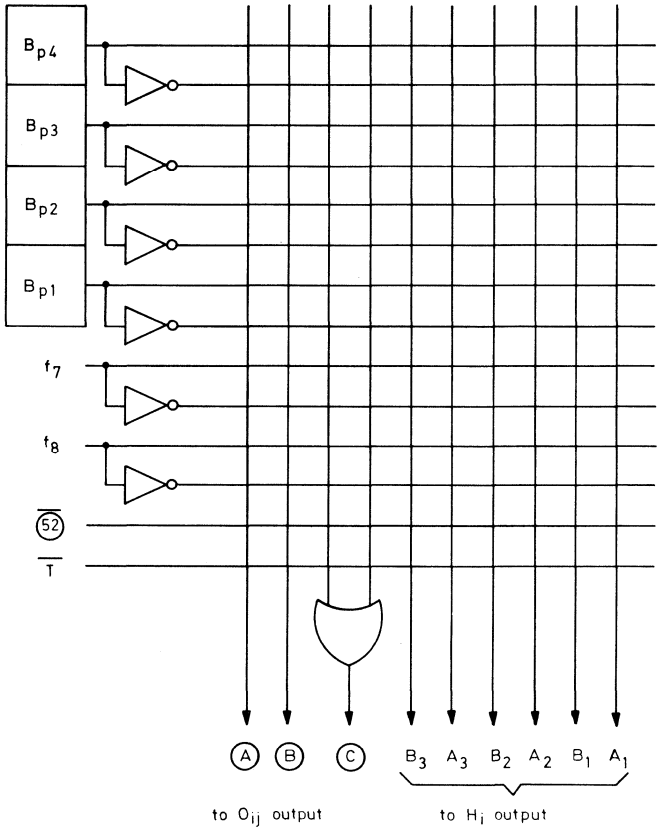


Fig. 8: Matrix construction of PLA1

4.6.2. PLA1

As shown in Fig. 8, PLA1 is a matrix with inputs from the B_p flip-flops and from internal signals. It controls the gates and buffers for the H_i and for the O_{ij} outputs. The matrix of PLA1 is constructed with AND gates. B_{p4} to B_{p1} means the contents of B_p flip-flops (the contents of the B_p flip-flops will be set by the ATBP instruction).

4.6.3. H_i Output Port (i = 1 to 3)

The outputs H_1 to H_3 are three-level controlled. GND level is logic 0, V_B level is logic 1, and the level V_M (half of the supply voltage V_B) is the third level. Fig. 9 shows the output levels of H_i as a function of the inputs A_i and B_i, where A_i and B_i are outputs of PLA1.

Caution: The SAA 6000 may be damaged if $A_i = 1$ and $B_i = 1$ are applied simultaneously.

A_i	B_i	H_i
0	0	V_M
0	1	0
1	0	1
1	1	prohibited

Fig. 9: H_i gate and buffer

4.6.4. Outputs O_{ij} (i = 1 to 4; j = 1 to 8) and O_{S1}, O_{S2}

W' and W are 8 static shift registers with a length of 9 bits each. The upper four shift registers W' can be accessed from the accumulator by the ATW and PATW instructions. It is also possible to connect the four W' registers in series in order to obtain one long shift register of 36 bits. The lower shift registers W can be loaded in parallel from the W' registers by the TW and PTW instructions.

Two bits, i.e. one bit of the upper and one bit of the lower shift registers, access one common O_{ij} output through the O_{ij} gate and buffer. This access is shown in Fig. 11.

T means the T flip-flop. It can be set for test purposes by the ST instruction and is resettable only by power off. In the test mode, with the T flip-flop set, jump instructions TR0 and TR1 are not executed if K_1 is at H level. Ⓐ, Ⓑ, and Ⓒ are the outputs of PLA1. ㊷ is an internal signal, generated during the execution of the READ or WRITE instruction.

4.7. I/O Port DIO

The 4-bit input-output port DIO is connected to the accumulator, both directly and through the F registers for output operations. The output buffers are tri-state controlled and become high-impedance when the levels supplied to the DIO pins are read into the accumulator. During the execution of the write instruction the contents of the accumulator are fed out through the DIO port for the time of one instruction cycle.

The contents of the F flip-flops are present on the DIO outputs at all times except during a READ or WRITE instruction.

4.8. Clock Generation

By connecting a crystal and two capacitors (Fig. 12), the clock signal may be generated on-chip. On the other hand, external clock drive is possible by driving O_{in} with a voltage having a low level of 0 to 0.3 V and a high level of $V_B - 0.3$ V to V_B.

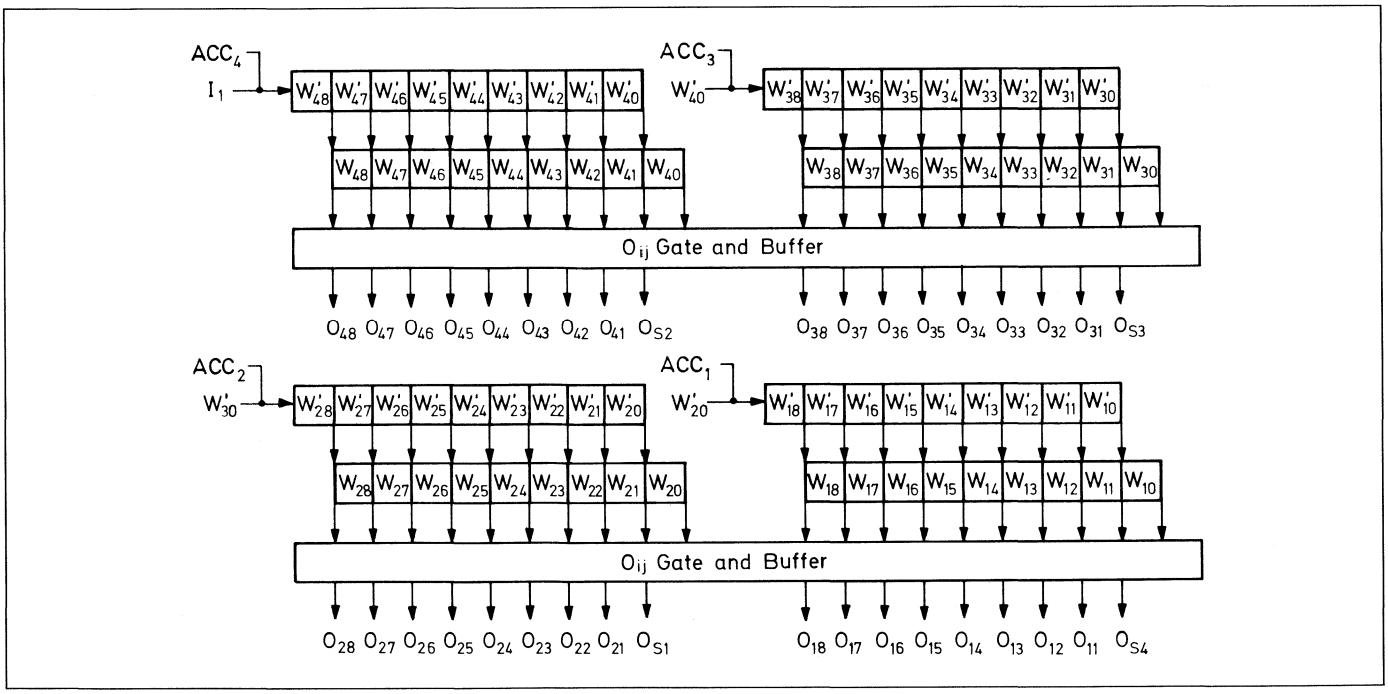


Fig. 10: Static shift registers W' and W

O_{48}	$((I_1 \wedge T) \vee (W'_{48} \wedge Ⓑ) \vee (W_{48} \wedge Ⓒ)) \oplus Ⓐ$
O_{38}	$((I_2 \wedge T) \vee (W'_{38} \wedge Ⓑ) \vee (W_{38} \wedge Ⓒ)) \oplus Ⓐ$
O_{28}	$((I_3 \wedge T) \vee (W'_{28} \wedge Ⓑ) \vee (W_{28} \wedge Ⓒ)) \oplus Ⓐ$
O_{18}	$((I_4 \wedge T) \vee (W'_{18} \wedge Ⓑ) \vee (W_{18} \wedge Ⓒ)) \oplus Ⓐ$
O_{47}	$((I_5 \wedge T) \vee (W'_{47} \wedge Ⓑ) \vee (W_{47} \wedge Ⓒ)) \oplus Ⓐ$
O_{37}	$((I_6 \wedge T) \vee (W'_{37} \wedge Ⓑ) \vee (W_{37} \wedge Ⓒ)) \oplus Ⓐ$
O_{27}	$((I_7 \wedge T) \vee (W'_{27} \wedge Ⓑ) \vee (W_{27} \wedge Ⓒ)) \oplus Ⓐ$
O_{17}	$((I_8 \wedge T) \vee (W'_{17} \wedge Ⓑ) \vee (W_{17} \wedge Ⓒ)) \oplus Ⓐ$
O_{46}	$((B_{M4} \wedge ⑤②) \vee (W'_{46} \wedge Ⓑ) \vee (W_{46} \wedge Ⓒ)) \oplus Ⓐ$
O_{36}	$((B_{M3} \wedge ⑤②) \vee (W'_{36} \wedge Ⓑ) \vee (W_{36} \wedge Ⓒ)) \oplus Ⓐ$
O_{26}	$((B_{M2} \wedge ⑤②) \vee (W'_{26} \wedge Ⓑ) \vee (W_{26} \wedge Ⓒ)) \oplus Ⓐ$
O_{16}	$((B_{M1} \wedge ⑤②) \vee (W'_{16} \wedge Ⓑ) \vee (W_{16} \wedge Ⓒ)) \oplus Ⓐ$
O_{45}	$((B_{L4} \wedge ⑤②) \vee (W'_{45} \wedge Ⓑ) \vee (W_{45} \wedge Ⓒ)) \oplus Ⓐ$
O_{35}	$((B_{L3} \wedge ⑤②) \vee (W'_{35} \wedge Ⓑ) \vee (W_{35} \wedge Ⓒ)) \oplus Ⓐ$
O_{25}	$((B_{L2} \wedge ⑤②) \vee (W'_{25} \wedge Ⓑ) \vee (W_{25} \wedge Ⓒ)) \oplus Ⓐ$
O_{15}	$((B_{L1} \wedge ⑤②) \vee (W'_{15} \wedge Ⓑ) \vee (W_{15} \wedge Ⓒ)) \oplus Ⓐ$
O_{ij} (i = 4 to 1; j = 4 to 1)	$((W'_{in} \wedge Ⓑ) \vee (W_{in} \wedge Ⓒ)) \oplus Ⓐ$ (i = 4 to 1; n = 4 to 1)
O_{S2}	$((W'_{40} \wedge Ⓑ) \vee (W_{40} \wedge Ⓒ)) \oplus Ⓐ$
O_{S3}	$((W'_{30} \wedge Ⓑ) \vee (W_{30} \wedge Ⓒ)) \oplus Ⓐ$
O_{S1}	$((W'_{20} \wedge Ⓑ) \vee (W_{20} \wedge Ⓒ)) \oplus Ⓐ$
O_{S4}	$((W'_{10} \wedge Ⓑ) \vee (W_{10} \wedge Ⓒ)) \oplus Ⓐ$

Fig. 11: O_{ij} output table

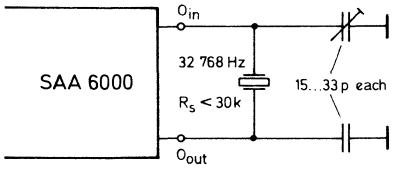


Fig. 12: External circuitry of the clock oscillator

4.9. Frequency Divider DIV

A resettable divider (DIV) or binary up counter of 15 stages (supplying the frequencies f_{16} to f_1) is connected to the accumulator ACC. The contents of the divider can be loaded into the accumulator by the DTA instruction. If the oscillator frequency is chosen to be 32 768 Hz, the frequencies f_{16} to f_1 can be found in the table Fig. 13.

f_{16}	32768 Hz	f_{12}	2048 Hz	f_8	128 Hz	f_4	8 Hz
f_{15}	16384 Hz	f_{11}	1024 Hz	f_7	64 Hz	f_3	4 Hz
f_{14}	8192 Hz	f_{10}	512 Hz	f_6	32 Hz	f_2	2 Hz
f_{13}	4096 Hz	f_9	256 Hz	f_5	16 Hz	f_1	1 Hz

Fig. 13: Output frequencies of the frequency divider DIV at 32768 Hz oscillator frequency

4.10. Standby Mode

The power consumption of the SAA 6000 can be reduced significantly by the use of the standby mode. This mode is entered after executing the CEND instruction. The internal clock is then stopped for all circuits on the chip except the clock generator, the 15-stage frequency divider, PLA1, PLA2 and the gate matrix for the H_i outputs. Thus the LCD can still be driven in the standby mode. Return to full operation mode is achieved by any of the following three signals:

a) L → H edge of the 1 s signal (f_1 output of DIV). Program flow starts at address (C_X, C_A, P_U, P_L) = 0, 0, 0, 0.
b) High level at any of the K_i inputs. Program flow starts at address (C_X, C_A, P_U, P_L) = 0, 0, 0, 0.
c) H → L edge at the ACL input. Program flow starts at address (C_X, C_A, P_U, P_L) = 0, 0, F, 0.

Before the standby mode is entered by means of CEND, the TS flip-flop must by reset (by a TIS instruction if necessary). This is required even if it is not intended to use the 1 second time-out to cause the return from the standby mode.

5. Programming Manual

5.1. Classification of the Instruction Set

The SAA6000 instruction set includes different types of instructions:

- RAM address instructions
- Data transfer and I/O instructions – move data between registers (including I/O registers) and memory and change the internal flags
- Arithmetic instructions
- Logical instructions – complement and rotate data
- Test instructions – conditional branches
- Special instructions
- ROM address instructions

5.2. Detailed Description of the Instructions

The following pages provide a detailed description of the instruction set of the SAA6000. Each instruction is described in the following manner:

1. The assembler format, consisting of the instruction mnemonic and operand fields, is printed in bold type at the left on the first line.
2. The full name of the instruction is included at the right on the first line(s).
3. The next line(s) contain a symbolic description of the operation of the instruction.
4. This is followed by a narrative description of the operation of the instruction.
5. The following line(s) contain on the left the binary code of the machine instruction, ending with the letter B, and on the right the hex code ending with the letter H.

In the descriptions of the operations it is implicit that transfers take place between corresponding bits of registers. Thus "(K_4 to K_1) → (ACC)" is to be interpreted as (K_4) → (ACC_4). (K_3) → (ACC_3). (K_2) → (ACC_2). (K_1) → (ACC_1).

I. RAM Address Instructions

1. SBM Set B_M

$1 \rightarrow (B_{M3})$

Sets B_{M3} to 1 for the next instruction only.

0000 0010B 02H

2. LB x, y Load B (short form)

$x \rightarrow (B_{L2,1})$. $y \rightarrow (B_{M2,1})$

where $x = I_4, I_3$ and $y = I_2, I_1$

Loads four least significant bits of the instruction word into least significant two bits of B_L and B_M. Bits 4 and 3 of B_M are unchanged. Bits 4 and 3 of B_L are set to 0,0 if $x = 0$ and to 1,1 if $x \neq 0$. Prepares for access (by subsequent instruction) to a limited area of RAM which is shown in Fig. 14. (See also Fig. 5).

0100 $I_4I_3I_2I_1$B 40H to 4FH

3. LBL x, y Load B (long form)

$x \rightarrow (B_M)$. $y \rightarrow (B_L)$

where $x = I_8$ to I_5 and $y = I_4$ to I_1 in second byte of instruction.

I_4	I_3	B_L
0	0	0
0	1	D
1	0	E
1	1	F

		B_M	
I_2	I_1	$B_{M3} = 0$	$B_{M3} = 1$
0	0	X	U
0	1	Y	T
1	0	Z	U
1	1	M	T

Fig. 14: Possible jump addresses for the LB x, y instruction

A two-byte instruction to load a value into B_L and B_M. Prepares for access (by subsequent instruction) to any part of RAM.

0101 1111B 5FH

$I_8I_7I_6I_5$ $I_4I_3I_2I_1$B 00H to FFH

4. INCB Increment B_L

$(B_L) + 1 \rightarrow (B_L)$. Skip if $(B_L) = a$

Increments the contents of register B_L by one. Skips next instruction if the contents of B_L then equal a (see section 5.6.).

0110 0100B 64H

5. DECB Decrement B_L

$(B_L) - 1 \rightarrow (B_L)$. Skip if $(B_L) = b$

Decrements the contents of register B_L by one. Skips next instruction if the contents of B_L then equal b (see section 5.6.).

0110 1100B 6CH

6. EXBLA Exchange B_L with ACC

$(B_L) \leftrightarrow (ACC)$

Exchanges contents of register B_L with the contents of the accumulator.

0000 1011B 0BH

II. Data Transfer and I/O Instructions

7. EXC x Exchange

$(ACC) \leftrightarrow ((B_L), (B_M))$

$(B_{M2,1}) \oplus x \rightarrow (B_{M2,1})$

where $x = I_2, I_1$

Exchanges the contents of the accumulator with the contents of a RAM word whose address is contained in the B_L and B_M registers. Loads exclusive OR function of the contents of $B_{M2,1}$ with x into $B_{M2,1}$.

0001 $00I_2I_1$B 10H to 13H

8. EXCI x Exchange and increment

$(ACC) \leftrightarrow ((B_L), (B_M))$

$(B_{M2,1}) \oplus x \rightarrow (B_{M2,1})$ where $x = I_2, I_1$

$(B_L) + 1 \rightarrow (B_L)$. Skip if $(B_L) = a$.

Exchanges the contents of the accumulator with the contents of a RAM word whose address is contained in the B_L and B_M registers. Loads exclusive OR function of the contents of $B_{M2,1}$ with x into $B_{M2,1}$. The contents of B_L are incremented by one. Skips next instruction if the contents of B_L then equal a (see section 5.6.).

0001 $01I_2I_1$B 14H to 17H

9. EXCD x Exchange and decrement

$(ACC) \leftrightarrow ((B_L), (B_M))$

$(B_{M2,1}) \oplus x \rightarrow (B_{M2,1})$, where $x = I_2, I_1$

$(B_L) - 1 \rightarrow (B_L)$. Skip if $(B_L) = b$

Exchanges the contents of the accumulator with the contents of a RAM word whose address is contained in the B_L and B_M

registers. Loads exclusive OR function of the contents of $B_{M2,1}$ with x into $B_{M2,1}$. The contents of B_L are decremented by one. Skips next instruction if the contents of B_L then equal b (see section 5.6.).
0001 $11I_2I_1$B 1CH to 1FH

10. LDA x Load ACC
$((B_L), (B_M)) \rightarrow (ACC)$
$(B_{M2,1}) \oplus x \rightarrow (B_{M2,1})$, where $x = I_2, I_1$
Loads the contents of the RAM word whose address is contained in the B_L and B_M registers into the accumulator. Loads exclusive OR function of the contents of $B_{M2,1}$ with x into $B_{M2,1}$.
0001 $10I_2I_1$B 18H to 1BH

11. LAX x Load immediate
$x \rightarrow (ACC)$, where $x = I_4I_3I_2I_1$
Loads x, the least significant 4 bits of the instruction code, into the accumulator. If several LAX x instructions follow one another, only the first LAX x instruction is executed and the following LAX x instructions are ignored.
0010 $I_4I_3I_2I_1$B 20H to 2FH

12. DTA DIV to ACC
$(DIV) \rightarrow (ACC)$
where I_2I_1 in the second instruction byte select the stages of DIV as shown in Fig. 15.

I_2	I_1	ACC_4	ACC_3	ACC_2	ACC_1
0	0	f_1	f_2	f_3	f_4
0	1	f_5	f_6	f_7	f_8
1	0	f_9	f_{10}	f_{11}	f_{12}
1	1	f_{13}	f_{14}	f_{15}	f_{16}

Fig. 15: Truth table for the data transfer $(DIV) \rightarrow (ACC)$

Loads the contents of four stages of the divider DIV into the accumulator. The four stages are selected by I_2I_1.
0101 1110B 5EH
**** $*1I_2I_1$B *4H to *7H; *CH to *FH

13. KTA K to ACC
$(K_4 \text{ to } K_1) \rightarrow (ACC)$
Loads the contents of K flip-flops into the accumulator.
0110 1010B 6AH

14. ATBP ACC to B_p
$(ACC) \rightarrow (B_{p4} \text{ to } B_{p1})$
Loads the contents of the accumulator into the B_p flip-flops.
0000 0001B 01H

15. WR Right shift W' with reset
$0 \rightarrow (W'_{48}) \rightarrow (W'_{47}) \rightarrow \ldots (W'_{40}) \rightarrow (W'_{38}) \rightarrow (W'_{37}) \rightarrow \ldots (W'_{30}) \rightarrow (W'_{28}) \rightarrow (W'_{27}) \rightarrow \ldots (W'_{20}) \rightarrow (W'_{18}) \rightarrow (W'_{17}) \rightarrow \ldots (W'_{10})$
Resets the contents of W'_{48}. Right shifts contents of W' registers.
0110 0010B 62H

16. WS Right shift W' with set
$1 \rightarrow (W'_{48}) \rightarrow (W'_{47}) \rightarrow \ldots (W'_{40}) \rightarrow (W'_{38}) \rightarrow (W'_{37}) \rightarrow \ldots (W'_{30}) \rightarrow (W'_{28}) \rightarrow (W'_{27}) \rightarrow \ldots (W'_{20}) \rightarrow (W'_{18}) \rightarrow (W'_{17}) \rightarrow \ldots (W'_{10})$
Sets the contents of W'_{48}. Right shifts contents of W' registers.
0110 0011B 63H

17. ATW ACC to W
$(ACC_4) \rightarrow (W'_{48}) \rightarrow (W'_{47}) \rightarrow \ldots (W'_{40})$
$(ACC_3) \rightarrow (W'_{38}) \rightarrow (W'_{37}) \rightarrow \ldots (W'_{30})$
$(ACC_2) \rightarrow (W'_{28}) \rightarrow (W'_{27}) \rightarrow \ldots (W'_{20})$
$(ACC_1) \rightarrow (W'_{18}) \rightarrow (W'_{17}) \rightarrow \ldots (W'_{10})$
Loads contents of the accumulator into upper bits of W' registers and right shifts contents of all four W' registers without carry from one register to the next.
0101 1101B 5DH

18. PATW Partially right shift, ACC to W
$(ACC_4) \rightarrow (W'_{48}) \rightarrow (W'_{47})$
$(ACC_3) \rightarrow (W'_{38}) \rightarrow (W'_{37})$
$(ACC_2) \rightarrow (W'_{28}) \rightarrow (W'_{27})$
$(ACC_1) \rightarrow (W'_{18}) \rightarrow (W'_{17})$
Loads contents of the accumulator into upper bits of W' registers and right shifts only upper two bits of all four W' registers.
0000 0000B 00H

19. ATF ACC to F
$(ACC) \rightarrow (F_4 \text{ to } F_1)$
Loads contents of the accumulator into F flip-flops.
0110 000B 60H

20. ATR ACC to R
$(ACC) \rightarrow (R_4 \text{ to } R_1)$
Loads contents of the accumulator into R flip-flops.
0110 0001B 61H

21. READ Read
$(DIO_4 \text{ to } DIO_1) \rightarrow (ACC)$
Loads conditions on DIO pins (treated as inputs) into accumulator.
0110 1000B 68H

22. WRITE Write
$(ACC) \rightarrow (DIO_4 \text{ to } DIO_1)$
Outputs contents of accumulator to DIO pins. The tri-state outputs are strobed by the ⑤② signal. This instruction therefore differs from ATF.
0110 1001B 69H

23. TW Transfer W' to W
$(W'_{in}) \rightarrow (W_{in})$, where $i = 1$ to 4; $n = 0$ to 8
Transfers contents of W' registers into W registers.
0101 1100B 5CH

24. PTW Partially transfer W' to W
$(W'_{im}) \rightarrow (W_{im})$, where $i = 1$ to 4; $m = 8, 7$
Transfers the contents of the top two bits of W' registers into top two bits of W registers.
0101 1001B 59H

25. IDIV Initialize divider
$0 \rightarrow (f_d)$, where $d = 1$ to 15
Resets all 15 stages of the divider.
0110 0101B 65H

26. RC Reset carry
$0 \rightarrow (C)$
Resets carry flip-flop.
0110 0110B 66H

27. SC Set carry
$1 \rightarrow (C)$
Sets carry flip-flop.
0110 0111B 67H

28. RM_p Reset memory bit
$0 \rightarrow ((B_L), (B_M))_p$, where $p = I_2, I_1$
Resets a bit of a RAM word whose address is contained in the B_L and B_M registers. The bit within this word is specified by the two least significant bits of the instruction word.
0000 $01I_2I_1$B 04H to 07H

29. SM_p Set memory bit
$1 \rightarrow ((B_L), (B_M))_p$, where $p = I_2, I_1$
Sets a bit of a RAM word whose address is contained in the B_L and B_M registers. The bit within this word is specified by the two least significant bits of the instruction word.
0000 $11I_2I_1$B 0CH to 0FH

III. Arithmetic Instructions

30. ADD Add
$((B_L), (B_M)) + (ACC) \rightarrow (ACC)$
The contents of the RAM word whose address is contained in the B_L and B_M registers are binary added to the contents of the accumulator. The result is placed in the accumulator. The carry flip-flop is not affected.
0000 1000B 08H

31. ADD 11 Add with carry
$((B_L), (B_M)) + (C) + (ACC) \rightarrow (ACC)$
$C_4 \rightarrow (C)$. Skip if $C_4 = 1$
The contents of the RAM word whose address is contained in the B_L and B_M registers and the contents of the C flip-flop are binary added to the contents of the accumulator. The result is placed in the accumulator and the carry flip-flop. The next instruction is skipped if a carry is generated.
0000 1001B 09H

32. ADX x Add immediate
$x + (ACC) \rightarrow (ACC)$, where $x = I_4$ to I_1
$C_4 \rightarrow (C)$. Skip if $C_4 = 1$
The four least significant bits of the instruction are binary added to the contents of the accumulator. The result is placed in the accumulator and the carry flip-flop. The next instruction is skipped if a carry is generated.
0011 $I_4I_3I_2I_1$B 30H to 39H, 3BH to 3FH

33. DC Add 10
$10_{10} + (ACC) \rightarrow (ACC)$
$C_4 \rightarrow (C)$. No skip.
10D = 1010B = AH is binary added to the contents of the accumulator. The result is placed in the accumulator and the carry flip-flop. It does not cause a skip. This is a special case of ADX x where $x = 10_{10}$.
0011 1010B 3AH

IV. Logical Instructions

34. COMA Complement ACC
$\overline{(ACC)} \rightarrow (ACC)$
The contents of the accumulator are complemented.
0000 1010B 0AH

35. ROT Rotate right through carry
$(C) \rightarrow (ACC_4) \rightarrow (ACC_3) \rightarrow (ACC_2) \rightarrow (ACC_1) \rightarrow (C)$
The contents of the accumulator are rotated right one position through the carry flip-flop. The high order bit of the accumulator is loaded with the contents of the carry flip-flop.
0110 1011B 6BH

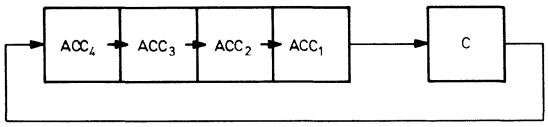


Fig. 16: Rotate right through carry

V. Test Instructions

These cause a skip of the next instruction byte, not the next instruction. If the following instruction is a two-byte instruction the second byte will then be executed as if it were an independent one byte instruction.

36. TA Test α
Skip if $(\alpha) = 1$. $0 \rightarrow (\alpha)$
Causes a skip of the next instruction byte if the contents of the α flip-flop equal 1; then resets α.
0101 0000B 50H

37. TB Test β
Skip if $(\beta) = 1$
Causes a skip of the next instruction byte if the contents of the β flip-flop equal 1.
0101 0001B 51H

38. TC Test carry
Skip if (C) = 0
Causes a skip of the next instruction byte if the contents of the carry flip-flop equal 0.
0101 0010B 52H

39. TAM Test ACC against memory
Skip if $(ACC) = ((B_L), (B_M))$
Causes a skip of the next instruction byte if the contents of the accumulator equal the contents of the RAM word whose address is contained in the B_L and B_M registers.
0101 0011B 53H

40. TM_p Test memory bit
Skip if $((B_L), (B_M))_p = 1$, where $p = I_2, I_1$
Causes a skip of the next instruction byte if the bit in the RAM word whose address is contained in the B_L and B_M registers equals 1. The bit within this word is specified by the two least significant bits of the instruction word.
0101 $01I_2I_1$B 54H to 57H

41. TA0 Test ACC for 0
Skip if (ACC) = 0
Causes a skip of the next instruction byte if the contents of the accumulator equal 0.
0101 1010B 5AH

42. TABL Test ACC against B_L

Skip if (ACC) = (B_L)

Causes a skip of the next instruction byte if the contents of the accumulator equal the contents of the B_L register.

0101 1011B 5BH

43. TIS Test 1 s signal

Skip if (TS) = 0

As shown in the timing diagram Fig. 17, the H → L edge of the f_1 signal (1 second signal) sets the TS flip-flop. The TIS instruction causes a skip of the next instruction byte if the TS flip-flop is reset. The TS flip-flop is reset after the execution of the TIS instruction.

0101 1000B 58H

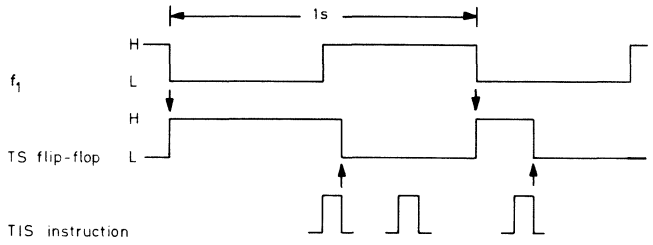


Fig. 17: Timing diagram for the TIS instruction

44. TAL Test low voltage alarm

Skip if (BA) = 1

Causes a skip of the next instruction byte if the BA pin is at 1, i.e. if the supply voltage is normal. (See section 4.5.3.)

0101 1110B 5EH

**** *010B *2H, *AH

VI. Special Instructions

45. CEND Clock end

→ Standby mode

Stops the system clock. For restarting conditions from the standby mode into the full operation mode see section 4.10.

0101 1110B 5EH

**** *000B *0H, *8H

46. ST Set T

1 → (T)

Sets T flip-flop. Used for testing purposes (see Fig. 11 and section 4.6.4). The T flip-flop is reset only by a power-on reset.

0101 1110B 5EH

**** *011B *3H, *BH

VII. ROM Address Instructions

47. ATPL ACC to P_L

(ACC) → (P_{L1} to P_{L4})

Loads the contents of the accumulator into the four least significant bits of the program counter P_L. P_{L6} and P_{L5} are unchanged.

0000 0011B 03H

48. COMCB Complement C_B

$\overline{(C_B)}$ → (C_B)

The contents of the C_B flip-flop are complemented.

0110 1101B 6DH

49. SSR x Load stack immediate

x → (S_U), where x = I_4 to I_1

1 → (E)

Loads the four least significant bits of the instruction word into the stack register S_U. Sets the E flip-flop which is reset automatically after the next instruction which will normally be TR0 x or TR1 x.

0111 $I_4I_3I_2I_1$B 70H to 7FH

50. TR0 x

if (G) = 0: x → (P_L), where x = I_6 to I_1
(S_U) → (P_U)
(C_B) → (C_A)

if (G) = 1: x → (P_L), where x = I_6 to I_1

Loads the six least significant bits of the instruction word into the program counter P_L. If the G flip-flop is reset, the contents of the stack register S_U are loaded into the program counter P_U and the contents of the C_B flip-flop are loaded into the C_A flip-flop. (The G flip-flop is set by TR1 and reset by the RTN0 or RTN1 instructions.)

10I_6I_5 $I_4I_3I_2I_1$B 80H to BFH

51. TR1 x

if (G) = 0, (E) = 0: x → (P_L), where x = I_6 to I_1
(P_U) → (S_U). 0 → (P_U)
(P_L) + 1 → (S_L)
(C_A) → (C_S). 1 → (C_A)
1 → (G).1 → (D)

if (G) = 0, (E) = 1: x → (P_L), where x = I_6 to I_1
(P_U) ↔ (S_U)
(P_L) + 1 → (S_L)
(C_A) → (C_S). (C_B) → (C_A)
1 → (G)

if (G) = 1: x_U → ($P_{U2,1}$), where x_U = I_6, I_5
except that if (C_X) = 1, (P_{U2}) is not affected
x_L → (P_{L4} to P_{L1}), where x_L = I_4 to I_1
0 → (P_{L6}, P_{L5})

If the G and the E flip-flops are both reset: Loads the six least significant bits of the instruction word into the program counter P_L. Loads the contents of the program counter P_U into the stack register S_U and then resets P_U. Loads the contents of P_L, incremented by one according to the polynomial code, into the stack register S_L. Loads the contents of C_A into C_S and sets the C_A, G and D flip-flops.

If the G flip-flop is reset and the E flip-flop is set: Loads the six least significant bits of the instruction word into the program counter P_L. Exchanges the contents of the program counter P_U with the contents of the stack register S_U. Loads the contents of P_L, incremented by one according to the polynomial code, into the stack register S_L. Loads the contents of C_A into C_S and the contents of C_B into C_A. Sets the G flip-flop.

If the G flip-flop is set: Loads the bits I_6 and I_5 of the instruction word into the two least significant bits of the program counter P_U in accordance with Fig. 21. If (C_X) equals 1, (P_{U2}) is not affected. Loads the four least significant bits of the instruction word into the four least significant bits of the program counter P_L. Resets the two most significant bits of P_L.

11I_6I_5 $I_4I_3I_2I_1$B C0H to FFH

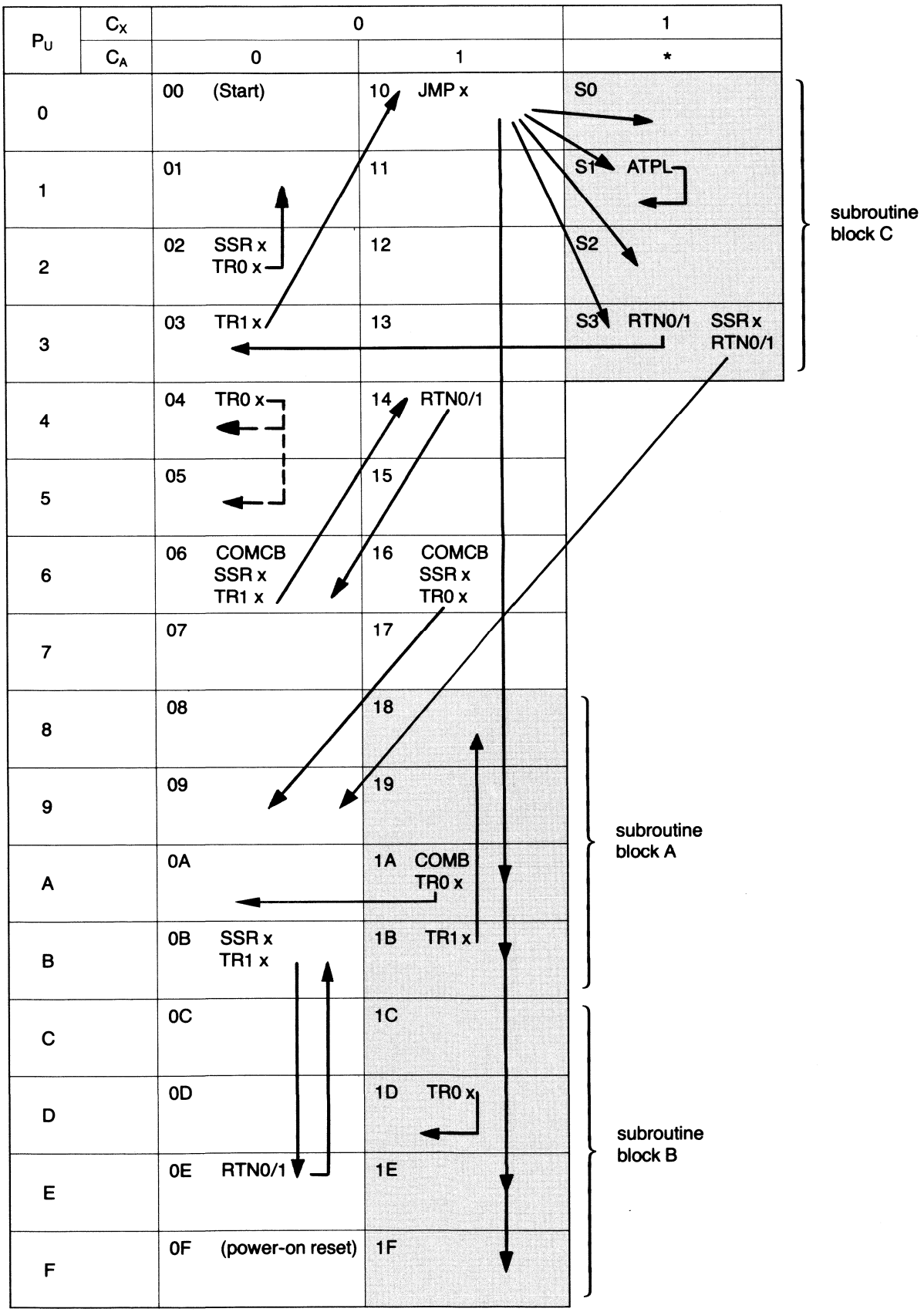


Fig. 18a: Examples of jump instructions

Subroutine Jumps			Other Jumps					
TR1 x	SSR x	COMCB	TR0 x	SSR x	COMCB	TR1 x	TR0 x	ATPL
JMP x	TR1 x	SSR x		TR0 x	SSR x			
.	.	TR1 x			TR0 x			
.	.	.						
RTN0/1	RTN0/1	.						
		RTN0/1						
			with (G) = 0			with (G) = 1		

Fig. 18b: Subroutine and non-subroutine jumps

52. RTN0 Return without skip

$(C_S) \rightarrow (C_A)$. $(S_U) \rightarrow (P_U)$
$(S_L) \rightarrow (P_L)$. $0 \rightarrow (G)$. $0 \rightarrow (C_X)$
Loads the contents of C_S, S_U and S_L into C_A, P_U and P_L respectively. Resets the G and the C_X flip-flops. This is a return from subroutine instruction.
0110 1111B 6EH

53. RTN1 Return with skip

$(C_S) \rightarrow (C_A)$. $(S_U) \rightarrow (P_U)$
$(S_L) \rightarrow (P_L)$. $0 \rightarrow (G)$. $0 \rightarrow (C_X)$
Skip the next instruction byte.
Loads the contents of C_S, S_U and S_L into C_A, P_U and P_L respectively. Resets the G and the C_X flip-flops and causes a skip of the next instruction byte. This is a return from subroutine instruction.
0110 1111B 6FH

54. JMP x Jump

If (D) = 1: $x_U \rightarrow (C_X)$, (P_U) as follows, where $x_U = I_8$ to I_6;
$\overline{I_8} \rightarrow (C_X)$. $I_8 \rightarrow (P_{U4})$
$I_8 \wedge I_7 \rightarrow (P_{U3})$. $I_8 \vee I_7 \rightarrow (P_{U2})$. $I_6 \rightarrow (P_{U1})$
$x_L \rightarrow (P_{L5}$ to $P_{L1})$, where $x_L = I_5$ to I_1
$0 \rightarrow (P_{L6})$. $0 \rightarrow$ (D)
This is not an independent instruction as it consists entirely of address bits for use by a TR1 x instruction elsewhere in the program. JMP x is executed if (D) = 1, i.e. if the TR1 x instruction is executed with (G) = 0, (E) = 0. JMP x causes a jump from page 10H to the designated page or subroutine page as shown in Fig. 20. The D flip-flop is reset after the execution of the JMP x instruction.
$I_8I_7I_6I_5$ $I_4I_3I_2I_1$B 00H to FFH

		(C_B)	(C_S)	(C_A)	(S_U)	(P_U)	(S_L)	(P_L)
1	TR1 x JMP x	–	(C_A)	1	(P_U)	see Fig. 20	$(P_L) + 1$	$0 \rightarrow (P_{L6})$ $x_{jL} \rightarrow (P_{L5...1})$
2	SSR x TR1 x	–	(C_A)	(C_B)	(P_U)	x_s	$(P_L) + 1$	x_t
3	COMCB SSR x TR1 x	$\overline{(C_B)}$	(C_A)	$\overline{(C_B)}$	(P_U)	x_s	$(P_L) + 1$	x_t
4	TR0 x [2])	–	–	(C_B)	–	(S_U)	–	x
5	SSR x TR0 x	–	–	(C_B)	x_s	x_s	–	x_t
6	COMCB SSR x TR0 x	$\overline{(C_B)}$	–	$\overline{(C_B)}$	x_s	x_s	–	x_t
7	TR1 x [1])	–	–	–	–	$x_U \rightarrow (P_{U2,1})$ see Fig. 21	–	$0,0 \rightarrow (P_{L6,5})$ $x_L \rightarrow (P_{L4...1})$
8	TR0 x [1])	–	–	–	–	–	–	x
9	ATPL	–	–	–	–	–	–	$(ACC) \rightarrow (P_{L4...1})$

Notes:
[1]) in subroutines only, i.e. with (G) = 1.
[2]) in main program only, i.e. with (G) = 0.
– means no change
x_j, x_s, x_t represent the x (= immediate) data contained in the JMP x, SSR x and TR0 x or TR1 x instructions, respectively.

Fig. 19: Contents of program counter after jump instruction or instruction sequence

5.3. Explanation of Jump Instructions

After a power-on reset, program execution starts at address (C_X, C_A, P_U, P_L) = 0, 0, F, 0. Stack registers S_U and S_L are not initialized by a power-on reset: they may be set by an SSR x, TR0 x sequence. The different types of jump instructions and instruction sequences are illustrated in Fig. 18. The contents of the various program counter and stack registers following the jump are listed in Fig. 19 in terms of the contents of those registers before the jump. Note that in all cases at least part of (P_L) is affected.
There is no "NO-OP" instruction as such for the SAA 6000, but the same effect can be achieved by means of a TR0 x instruction (or a TR1 x if (G) = 1) jumping to the next step.

Subroutine jumps.
These are defined as jumps in which (P_U), (P_L) are stacked, i.e. transferred to (S_U, S_L), to be unstacked later by a RTN0 or RTN1 instruction. The subroutine pages S0...S3 are not necessarily used. Besides pages S0 to S3, the eight pages 18 to 1F are also treated specially where jumps are concerned. These twelve pages may be regarded as being organized into three blocks of four pages each, as indicated in Fig. 18, for the purposes of certain jumps. However, Fig. 18 shows that subroutine jumps may be performed to any page. While in the subroutine mode, (G) will be 1.

1. TR1 x
   JMP x
The TR1 x instruction here performs a jump to page 10H, and the JMP x causes a jump to a designated page in accordance with Fig. 20. This sequence is the only way of jumping to one of the pages S0 to S3 from a non-subroutine page.

			Program counter after JMP x					Jumps
I_8	I_7	I_6	(C_X)	(P_{U4} to P_{U1})				to page
0	0	0	1	0	0	0	0	S0
0	0	1	1	0	0	0	1	S1
0	1	0	1	0	0	1	0	S2
0	1	1	1	0	0	1	1	S3
1	0	0	0	1	0	1	0	1A
1	0	1	0	1	0	1	1	1B
1	1	0	0	1	1	1	0	1E
1	1	1	0	1	1	1	1	1F

Fig. 20: Truth table for the JMP x instruction

2. SSR x
   TR1 x
This sequence performs a subroutine jump between two pages without changing the contents of C_X or C_A.

3. COMCB
   SSR x
   TR1 x
This sequence is the same as SSR x, TR1 x except that the contents of C_A are inverted.

Use of RTN0/RTN1 Instructions
If a subroutine program extends beyond a page boundary it must end with a jump (by a single TR1 x) back to the page where it started, and only then can the RTN0/RTN1 be used. In other words, the RTN0/RTN1 instruction must always be on the same page as the start of the subroutine, even if a jump or jumps to other pages are included in the subroutine.
The sequence

SSR x	or	SSR x
. . . .		. . . .
RTN0		RTN1

may be used to modify a return address, e.g. to create multiple return adresses.

Non-subroutine jumps.

4. TR0 x (in main program pages only, i.e. with (G) = 0)
This instruction jumps to any step within the same page. Depending on the contents of S_U before the jump, there may also be a change of page.

5. SSR x
   TR0 x
This sequence jumps to another page without changing (C_X) or (C_A). It is not used while in the subroutine mode because, when (G) = 1, TR0 x does not unstack the value loaded into S_U by SSR x. In the subroutine mode, therefore, the SSR x would be ineffective.

6. COMCB
   SSR x
   TR0 x
This sequence is the same as the above except that the contents of C_A are inverted.

7. TR1 x (in subroutines only, i.e. with (G) = 1)
This instruction causes a jump between subroutine pages as indicated in Fig. 21.

I_6	I_5	previous page				page after jump
*	0	S0	S1			S0
*	1	S0	S1			S1
*	0	S2	S3			S2
*	1	S2	S3			S3
0	0	18	19	1A	1B	18
0	1	18	19	1A	1B	19
1	0	18	19	1A	1B	1A
1	1	18	19	1A	1B	1B
0	0	1C	1D	1E	1F	1C
0	1	1C	1D	1E	1F	1D
1	0	1C	1D	1E	1F	1E
1	1	1C	1D	1E	1F	1F

Fig. 21: TR1 x subroutine jumps with (G) = 1

8. TR0 x (in subroutines only, i.e. with (G) = 1)
This instruction jumps within a page only.

9. ATPL
This instruction jumps within a page only. As it jumps to one of a number of locations depending on the contents of the accumulator, it is useful in accessing look-up tables.

10. COMCB
    TR0 x
This sequence jumps between two pages having the same P_U value but in different fields (with (G) = 0).

5.4. Table of the SAA 6000 Instruction Set

Mnemonic	Code	Micro Instruction
I. RAM Address Instructions		
DECB	0110 1100	$(B_L) - 1 \rightarrow (B_L)$. Skip if $(B_L) = b$
EXBLA	0000 1011	$(B_L) \leftrightarrow (ACC)$
INCB	0110 0100	$(B_L) + 1 \rightarrow (B_L)$. Skip if $(B_L) = a$
②LBL x, y	0101 1111 $I_8I_7I_6I_5$ $I_4I_3I_2I_1$	I_8 to $I_5 \rightarrow (B_{M4}$ to $B_{M1})$. I_4 to $I_1 \rightarrow (B_{L4}$ to $B_{L1})$
LB x, y	0100 $I_4I_3I_2I_1$	$I_4, I_3 \rightarrow (B_{L2,1})$. $I_2, I_1 \rightarrow (B_{M2,1})$
SBM	0000 0010	$1 \rightarrow (B_{M3})$ for next step only
II. Data Transfer and I/O Instructions		
ATBP	0000 0001	$(ACC) \rightarrow (B_p)$
ATF	0110 0000	$(ACC) \rightarrow (F)$
ATR	0110 0001	$(ACC) \rightarrow (R)$
ATW	0101 1101	$(ACC) \rightarrow (W'_{i8})$ (i = 1 to 4). Right shift W'_{in} (i = 1 to 4; n = 7 to 0)
②DTA	0101 1110 **** *1I_2I_1	$(DIV) \rightarrow (ACC)$
EXCD x	0001 11I_2I_1	$(ACC) \leftrightarrow ((B_L), (B_M))$. $(B_{M2,1}) \oplus I_2, I_1 \rightarrow (B_{M2,1})$. $(B_L) - 1 \rightarrow (B_L)$. Skip if $(B_L) = b$
EXCI x	0001 01I_2I_1	$(ACC) \leftrightarrow ((B_L), (B_M))$. $(B_{M2,1}) \oplus I_2, I_1 \rightarrow (B_{M2,1})$. $(B_L) + 1 \rightarrow (B_L)$. Skip if $(B_L) = a$
EXC x	0001 00I_2I_1	$(ACC) \leftrightarrow ((B_L), (B_M))$. $(B_{M2,1}) \oplus I_2, I_1 \rightarrow (B_{M2,1})$
IDIV	0110 0101	$0 \rightarrow (DIV)$
KTA	0110 1010	$(K) \rightarrow (ACC)$
LAX x	0010 $I_4I_3I_2I_1$	I_4 to $I_1 \rightarrow (ACC)$
LDA x	0001 10I_2I_1	$((B_L), (B_M)) \rightarrow (ACC)$. $(B_{M2,1}) \oplus I_2I_1 \rightarrow (B_{M2,1})$
PATW	0000 0000	$(ACC) \rightarrow (W'_{i8}) \rightarrow (W'_{i7})$ (i = 1 to 4)
PTW	0101 1001	$(W'_{im}) \rightarrow (W_{im})$ (i = 1 to 4; m = 8, 7)
RC	0110 0110	$0 \rightarrow (C)$
READ	0110 1000	$(DIO) \rightarrow (ACC)$
RM_p	0000 01I_2I_1	$0 \rightarrow ((B_L), (B_M))_p$, where $p = I_2, I_1$
SC	0110 0111	$1 \rightarrow (C)$
SM_p	0000 11I_2I_1	$1 \rightarrow ((B_L), (B_M))_p$, where $p = I_2, I_1$
TW	0101 1100	$(W'_{in}) \rightarrow (W_{in})$ (i = 1 to 4; n = 0 to 8)
WR	0110 0010	$0 \rightarrow (W'_{48})$, right shift W'_{in}
WRITE	0110 1001	$(ACC) \rightarrow (DIO)$
WS	0110 0011	$1 \rightarrow (W'_{48})$, right shift W'_{in}
III. Arithmetic Instructions		
ADD	0000 1000	$((B_L), (B_M)) + (ACC) \rightarrow (ACC)$
ADD 11	0000 1001	$((B_L), (B_M)) + (C) + (ACC) \rightarrow (ACC)$. $C_4 \rightarrow (C)$. Skip if $C_4 = 1$
ADX x	0011 $I_4I_3I_2I_1$	$I_{4,3,2,1} + (ACC) \rightarrow (ACC)$. $C_4 \rightarrow (C)$. Skip if $C_4 = 1$
DC	0011 1010	$10_{10} + (ACC) \rightarrow (ACC)$. $C_4 \rightarrow (C)$. No skip

Mnemonic	Code	Micro Instruction
IV. Logical Instructions		
COMA	0000 1010	$\overline{(ACC)} \rightarrow (ACC)$
ROT	0110 1011	$(C) \rightarrow (ACC_4) \rightarrow (ACC_3) \rightarrow (ACC_2) \rightarrow (ACC_1) \rightarrow (C)$
V. Test Instructions		
TA	0101 0000	Skip if $(\alpha) = 1$. $0 \rightarrow (\alpha)$
TA0	0101 1010	Skip if (ACC) = 0
TABL	0101 1011	Skip if (ACC) = (B_L)
②TAL	0101 1110 **** *010	Skip if (BA) = 1
TAM	0101 0011	Skip if (ACC) = $((B_L), (B_M))$
TB	0101 0001	Skip if $(\beta) = 1$
TC	0101 0010	Skip if (C) = 0
TIS	0101 1000	Skip if (TS) = 0
TM_p	0101 $01I_2I_1$	Skip if $((B_L), (B_M))_p = 1$, where $p = I_2, I_1$
VI. Special Instructions		
②CEND	0101 1110 **** *000	→ Standby
②ST	0101 1110 **** *011	$1 \rightarrow (T)$
VII. ROM Address Instructions		
ATPL	0000 0011	$(ACC) \rightarrow (P_{L1}$ to $P_{L4})$
COMCB	0110 1101	$\overline{(C_B)} \rightarrow (C_B)$
SSR x	0111 $I_4I_3I_2I_1$	I_4 to $I_1 \rightarrow (S_{U4}$ to $S_{U1})$. $1 \rightarrow (E)$

TR0 x	10I_6I_5 $I_4I_3I_2I_1$	if (G) = 0:
		I_6 to $I_1 \rightarrow (P_{L6}$ to $P_{L1})$. $(S_U \rightarrow P_U)$. $(C_B) \rightarrow (C_A)$.
		if (G) = 1:
		I_6 to $I_1 \rightarrow (P_{L6}$ to $P_{L1})$.

TR1 x	11I_6I_5 $I_4I_3I_2I_1$	if (G) = 0, (E) = 0:
		I_6 to $I_1 \rightarrow (P_{L6}$ to $P_{L1})$. $(P_U) \rightarrow (S_U)$. $0 \rightarrow (P_U)$. $(P_L) + 1 \rightarrow (S_L)$. $(C_A) \rightarrow (C_S)$.
		$1 \rightarrow (C_A)$. $1 \rightarrow (G)$. $1 \rightarrow (D)$
		if (G) = 0, (E) = 1:
		I_6 to $I_1 \rightarrow (P_{L6}$ to $P_{L1})$. $(P_U) \leftrightarrow (S_U)$. $1 \rightarrow (G)$. $(P_L) + 1 \rightarrow (S_L)$.
		$(C_A) \rightarrow (C_S)$. $(C_B) \rightarrow (C_A)$
		if (G) = 1:
		$I_{6,5} \rightarrow (P_{U2,1})$ except that (P_{U2}) is not affected if $(C_X) = 1$. I_4 to $I_1 \rightarrow (P_{L4}$ to $P_{L1})$. $0 \rightarrow (P_{L6,5})$

RTN0	0110 1110	$(C_S) \rightarrow (C_A)$. $(S_U) \rightarrow (P_U)$. $(S_L) \rightarrow (P_L)$. $0 \rightarrow (G)$. $0 \rightarrow (C_X)$
RTN1	0110 1111	$(C_S) \rightarrow (C_A)$. $(S_U) \rightarrow (P_U)$. $(S_L) \rightarrow (P_L)$. $0 \rightarrow (G)$. $0 \rightarrow (C_X)$. Skip
JMP	$I_8I_7I_6I_5$ $I_4I_3I_2I_1$	if (D) = 1: $\overline{I_8} \rightarrow (C_X)$. $I_8 \rightarrow (P_{U4})$. $I_8 \wedge I_7 \rightarrow (P_{U3})$. $I_8 \vee I_7 \rightarrow (P_{U2})$. $I_6 \rightarrow (P_{U1})$ I_5 to $I_1 \rightarrow (P_{L5}$ to $P_{L1})$. $0 \rightarrow (P_{L6})$. $0 \rightarrow (D)$

Notes: * means redundancy. ②LBL, ②DTA, ②TAL, ②CEND, and ②ST are two-byte instructions.

5.5. SAA 6000 Instruction Map

Hex codes Upper half-byte

Lower half-byte →

↓	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	18	14	1	47	28	28	28	28	30	31	34	6	29	29	29	29
1	7	7	7	7	8	8	8	8	10	10	10	10	9	9	9	9
2	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11
3	32	32	32	32	32	32	32	32	32	32	33	32	32	32	32	32
4	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
5	36	37	38	39	40	40	40	40	43	24	41	42	23	17	Note 2	
6	19	20	15	16	4	25	26	27	21	22	13	35	5	48	52	53
7	49	49	49	49	49	49	49	49	49	49	49	49	49	49	49	49
8	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50
9	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50
A	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50
B	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50
C	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51
D	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51
E	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51
F	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51

Notes:
1. The numbers in the map are those used in the full listing of the instructions in section 5.2.
2. 5EH is used for the first byte of instructions 12, 44, 45 and 46. 5FH is used for the first byte of instruction 3.

Fig. 22: Instruction map

5.6. Firmware Skip Conditions

The instructions INCB, DECB, EXCI x and EXCD x include a skip of the next instruction byte if the contents of the RAM address register B_L equal a or b (as appropriate). These skip conditions are constants, in the range of 0 to F (hexadecimal), programmed into the ROM. Two values may be programmed for a: in this case INCB and EXCI x will cause a skip if (B_L) is equal to either of the two values of a. Only one value may be programmed for b.

5.7. Execution of Instructions with Skips

When any of the test instructions or another instruction with a skip is executed and skip condition is not satisfied, the following instruction is fetched but is executed as a "NO-OP", i.e. the following instruction only creates a 60 μs delay. This should be noted when using skip-condition instructions in timing loops.

6. Application Notes

6.1. LCD Drive

An LCD can be driven directly by the SAA 6000. Using 2-phase multiplexing, the LCD may have up to 8 digits plus 4 special signs. Fig. 23 illustrates how an 8-digit 2-phase multiplexed LCD can be driven by the SAA 6000. The backplate of the display is split into two parts, which are connected to the outputs H_1 and H_2. In this example the partitioning is done such that each of the digits is split into two parts. PLA1 is set up in such a way (Fig. 28) that H_1 and H_2 supply a three-level signal during the display mode. The signals at H_1 and H_2 have the same waveform, but there is a 90° phase difference between them.

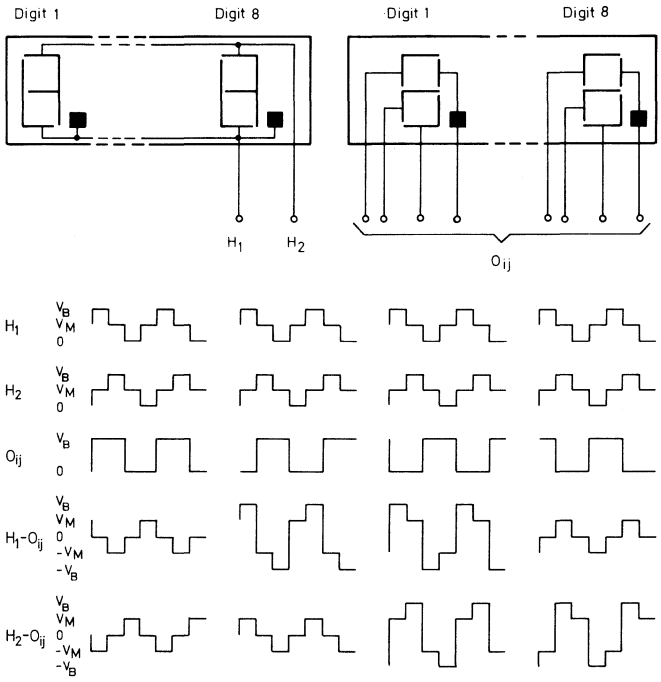


Fig. 23: LCD drive, using 2-phase multiplexing

Two segments, one from each of the two parts, are connected to one common pin. The signal applied to this pin comes from an O_{ij} output. The signals at the segments are the difference between the signals applied to their backplates and the O_{ij} signals. The last two pulse trains in Fig. 23 show these differences $H_1 - O_{ij}$ and $H_2 - O_{ij}$.

Four cases are shown. In the far left column H_1 is in phase with O_{ij}. The differences $H_1 - O_{ij}$ and $H_2 - O_{ij}$ result in signals with the same waveform and an amplitude of ±1.5 V.

In the second column from the left there is a phase difference between H_1 and O_{ij} of 90°. Now the signal $H_1 - O_{ij}$ has an amplitude of ±3 V while $H_2 - O_{ij}$ still has an amplitude of ±1.5 V.

In the third column from the left there is a phase difference between H_1 and O_{ij} of 180°. $H_1 - O_{ij}$ and $H_2 - O_{ij}$ here result in signals with an amplitude of ±3 V.

And finally, shown in the far right column, there is a phase difference between H_1 and O_{ij} of 270°. $H_1 - O_{ij}$ results in a signal

with an amplitude of ± 1.5 V and $H_2 - O_{ij}$ has an amplitude of ± 3 V.

The threshold voltage of the LCD has to be chosen such that the LCD is switched off when a signal with an amplitude of ± 1.5 V is applied, and switched on when the amplitude is ± 3 V. Thus the two segments connected to one common pin can both be switched off (first column) or one of them is switched on and the other one is switched off (second and fourth column), or both are switched on (third column).

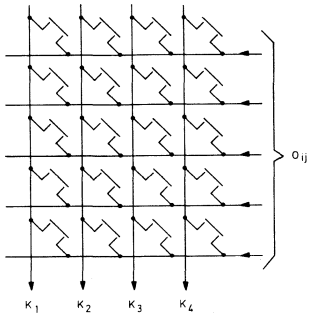
This control is provided completely by the hardware of the SAA 6000. All the program has to do is to load the shift registers whenever the displayed data has to be changed.

6.2. Keyboard Scanning

Fig. 24 illustrates how the O_{ij} outputs can be used for scanning a keyboard which is arranged in matrix form with columns and rows. The four columns are connected to the K_i inputs and the rows to the O_{ij} outputs. This example uses only five of 34 possible rows. The contacts short-circuit a row to a column.

The first step of the scanning routine checks whether any of the contacts is closed, by applying 1 to all O_{ij} outputs. The K_i inputs have internal pull-down resistors, being at logic 0 when no contact is closed.

The subsequent steps determine which key is pushed. This is done by applying 1 sequentially to one O_{ij} output at a time, all other O_{ij} outputs being at logic 0. After each step the information at the K_i inputs is transferred to the accumulator by the KTA instruction.



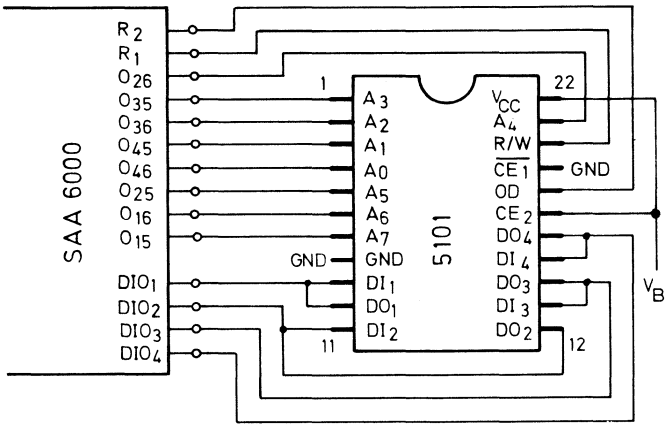
	Step					
	1	2	3	4	5	6
	1	1	0	0	0	0
	1	0	1	0	0	0
	1	0	0	1	0	0
	1	0	0	0	1	0
	1	0	0	0	0	1

Fig. 24: Keyboard scanning

6.3. External RAM Drive

Fig. 25 illustrates how to drive an external RAM of 256 x 4 bits with the SAA 6000. The registers B_L and B_M, addressing the internal RAM of the SAA 6000, here also address the external RAM through eight O_{ij} outputs (see also Fig. 11). The data bus is connected with the 4-bit I/O port DIO. PLA2 is set up such that R_1 controls the read/write function and R_2 disables the RAM outputs during the execution of the WRITE instruction (Fig. 26). The R_3 and R_4 flip-flops are connected directly with the outputs R_3 and R_4 respectively.

The external RAM can be expanded in blocks of 1 K bits by using outputs of the SAA 6000 as chip selects.



RAM DATA	DIO_1 to DIO_4
RAM ADDRESS	O_{ij} (i = 1 to 4; j = 5, 6)
RAM CONTROL	R_1, R_2

Fig. 25: External RAM drive

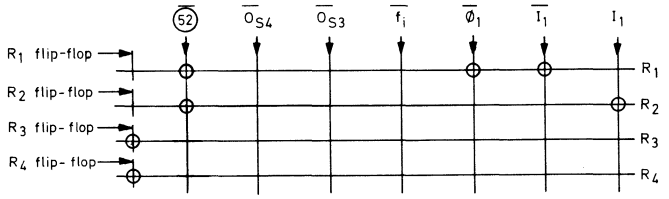


Fig. 26: PLA2 set up for external RAM drive and direct output of R_3 F/F and R_4 F/F

6.4. Multiplexing the O_{ij} Outputs

Fig. 27 illustrates how the O_{ij} outputs can be used for different purposes in a kind of time-sharing. A keyboard of up to 34 x 4 keys, an 8-digit LCD and a 1 K bit RAM are connected to the 34 O_{ij} outputs. Thus one O_{ij} output controls up to three different devices.

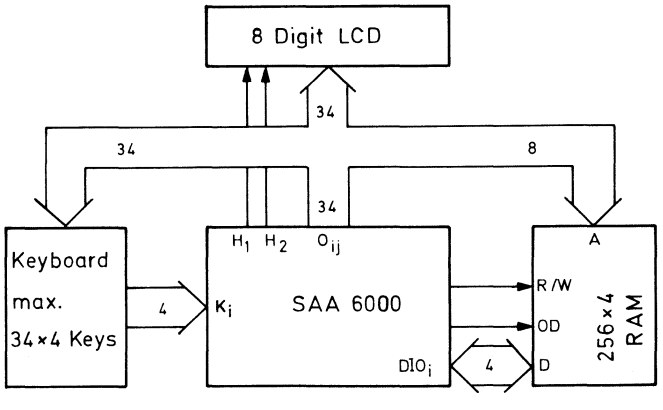


Fig. 27: Block diagram for multiplexing the O_{ij} outputs

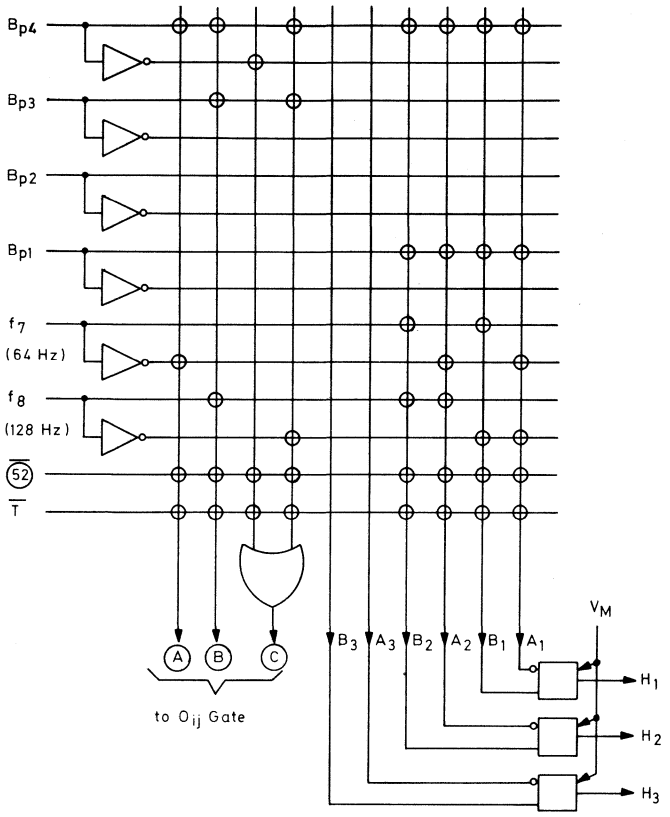


Fig. 28: Matrix example for PLA1 (AND gates)

The organization of PLA1 for this time-sharing is shown in Fig. 28 and the corresponding pulse train in Fig. 29. The four B_p flip-flops and the signal ⑤② determine which of the three devices is accessed. In the display mode, when $(B_{p1,3,4}) = 1,1,1$ and $\overline{52} = 1$, H_1 and H_2 generate 3-level a.c. signals to the backplate of the LCD. By means of the signals Ⓑ and Ⓒ the registers W' and W alternately have access to the O_{ij} outputs. Ⓐ periodically inverts the O_{ij} signals, in synchronism with the signals H_1 and H_2 for the backplates. For other microcomputers this is normally done externally with two-input exclusive OR gates, one gate for each segment pin.

During the scanning of the keyboard or the accessing of the external RAM the display is blanked by keeping H_1 and H_2 at the V_M level.

Mode	Display	Key scanning	Ext. RAM access
f_7 (64 Hz)	1 0		
f_8 (128 Hz)	1 0		
B_{P4}	1 1 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	* * * * * * * *
B_{P3}	1 1 1 1 1 1 1 1 1 1 1 1	* * * * * * * *	* * * * * * * *
B_{P2}	* * * * * * * * * * * *	* * * * * * * *	* * * * * * * *
B_{P1}	1 1 1 1 1 1 1 1 1 1 1 1	* * * * * * * *	* * * * * * * *
52	1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0
H_1	V_B 0		
H_2	V_B V_M 0		
A	1 0		
B	1 0		
C	1 0		
Access to O_{ij} outputs	W W' W W' W W' W W' W W' W W'	W	B_L, B_M for O_{ij} outputs where i = 1...4 and j = 5,6

Fig. 29: Timing diagram for multiplexing the O_{ij} outputs (* = redundant code)

7. Abbreviations and Symbols used in this Data Sheet

7.1. Abbreviations for Hardware Blocks

ACC	Accumulator
ACL	Automatic clear after supplying power to the SAA6000
ALU	Arithmetic logic unit
B_L, B_M	4-bit registers addressing internal and external RAM
B_p	4-bit register controlling PLA1
C	Carry flag
C_A	1-bit register of the program counter for field selection
C_B	1-bit preparation register for C_A, used for field jumps
CG	Clock generator
C_S	1-bit stack register for C_A
C_X	1-bit register of the program counter, defining the subroutine field
D	1-bit register, controlled by the ROM address instructions
DIV	15-stage frequency divider
E	1-bit register, controlled by the ROM address instructions
F	4-bit output register for the DIO port
f_d	15 stages of the frequency divider DIV
G	1-bit register, marking subroutine mode, controlled by the ROM address instructions
K	4-bit register for the K_1 to K_4 inputs
PC	Program counter
P_L	6-bit polynomial program counter
PLA1, PLA2	Programmable logic arrays
P_U	4-bit register of the program counter, defining the pages
R_1 to R_4	4-bit register for the R_1 to R_4 outputs, also controlling the PLA2
RAM	Random access memory (data memory)
ROM	Read only memory (program memory)
S_L	6-bit stack register for P_L
S_U	4-bit stack register for P_U
T	1-bit register for testing the ROM contents
TS	1-bit register, set by the H → L edge of the 1 s signal f_1 of the frequency divider DIV and read by the TIS instruction
W, W'	9-bit shift register
α, β	1-bit asynchronous inputs

7.2. Abbreviations for Signal Names

Ⓐ, Ⓑ, Ⓒ	Internal signals, generated by PLA1
C_4	Carry bit, generated by an addition with bit 4 of the accumulator
f_1 to f_{16}	16 frequencies supplied from the frequency divider DIV
f_i	A signal generated by a logical interconnection of three f_d outputs of the frequency divider DIV. $f_i = \overline{f_1 \wedge f_4 \wedge f_{13}}$
I_1 to I_8	8 bits of the instruction byte addressed by the program counter
OD	A signal at output R_2, used as output disable for an external RAM
R/W	A signal at output R_1, used as read/write for an external RAM
Φ_1, Φ_2	Phase 1 and 2 of the internal 2-phase clock
㊿	An internal signal, generated during the execution of the READ and WRITE instruction

7.3. Symbols

( )	The contents of a memory location or of a register enclosed in the parentheses
((B_L), (B_M))	The contents of the RAM word addressed by the contents of B_L, B_M
→	"is transferred to"
↔	"is exchanged with"
+	Addition
−	Subtraction
∧	Logical AND
∨	Logical OR
⊕	Logical exclusive OR
———	The one's complement (e.g. $\overline{(A)}$)

Contents

1. Introduction

The SAA 6002 – a mask-programmed version of the 4-bit one-chip microcomputer SAA 6000 – is intended for the design of an intelligent pushbutton telephone subset for pulse dialling. The wide range of operating features depends on the flexibility and extremely low current consumption of the SAA 6000 which is designed in low-threshold CMOS technology. The supply voltage is 3 V and the current consumption 15 to 45 μA depending on the mode of operation.

The SAA 6000 contains on a single silicon chip of a few square millimeters area a 2268 byte ROM, a RAM of 96 words with 4 bits each, 8 static shift registers with 9 bits each, a 15-stage frequency divider, the clock oscillator, ALU and accumulator, programmable logic arrays (PLA), and other logic circuits; see Fig. 2. Due to its extremely flat construction – 2 mm in height – the SAA 6000 is suited for application in equipment no thicker than a pocket notebook. Some of the typical application examples are:

– programmable IR transmitters for cordless remote control
– auto dialler for intelligent pushbutton telephone subsets
– taximeters
– clock calculators
– precision clocks
– stop watches
– cash registers
– vending machines
– controllers for various home electric appliances
– heart-rate monitors
– drivers for LCDs
– hand-held instruments (thermometers etc.)
– controllers for toys and games

In addition, upon the customer's request, many other applications are available.

1.1. Features of the SAA 6000:

– complete one-chip microcomputer
– ROM capacity : 2268 bytes
– RAM capacity : 96 words of 4 bits each
– instruction set : 54 instructions
– subroutine level : 1 level
– input port K input : 4 bits
– asynchronous input : 2 bits
– output port O_{ij} : 34 bits
H_i : 3 bits
R_i : 4 bits
– input/output port DIO : 4 bits
– divider of 15 stages with reset
– internal LCD drive circuit
– external RAM drive
– internal crystal oscillator circuit
– extremely small power consumption
– internal low-voltage detection circuit
– 60 pin quad package

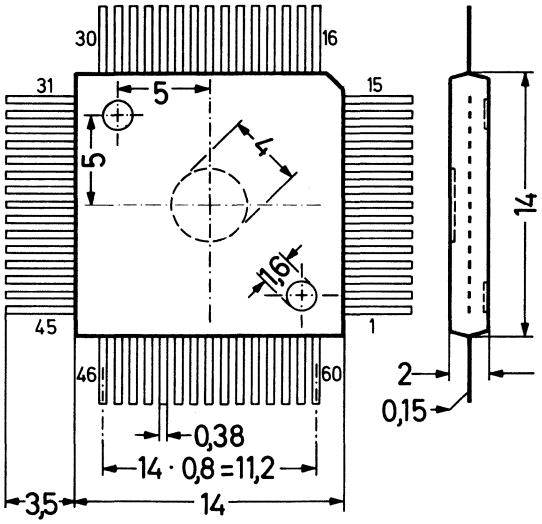


Fig. 1: SAA 6000 in plastic package
Weight approx. 0.8 g
Dimensions in mm

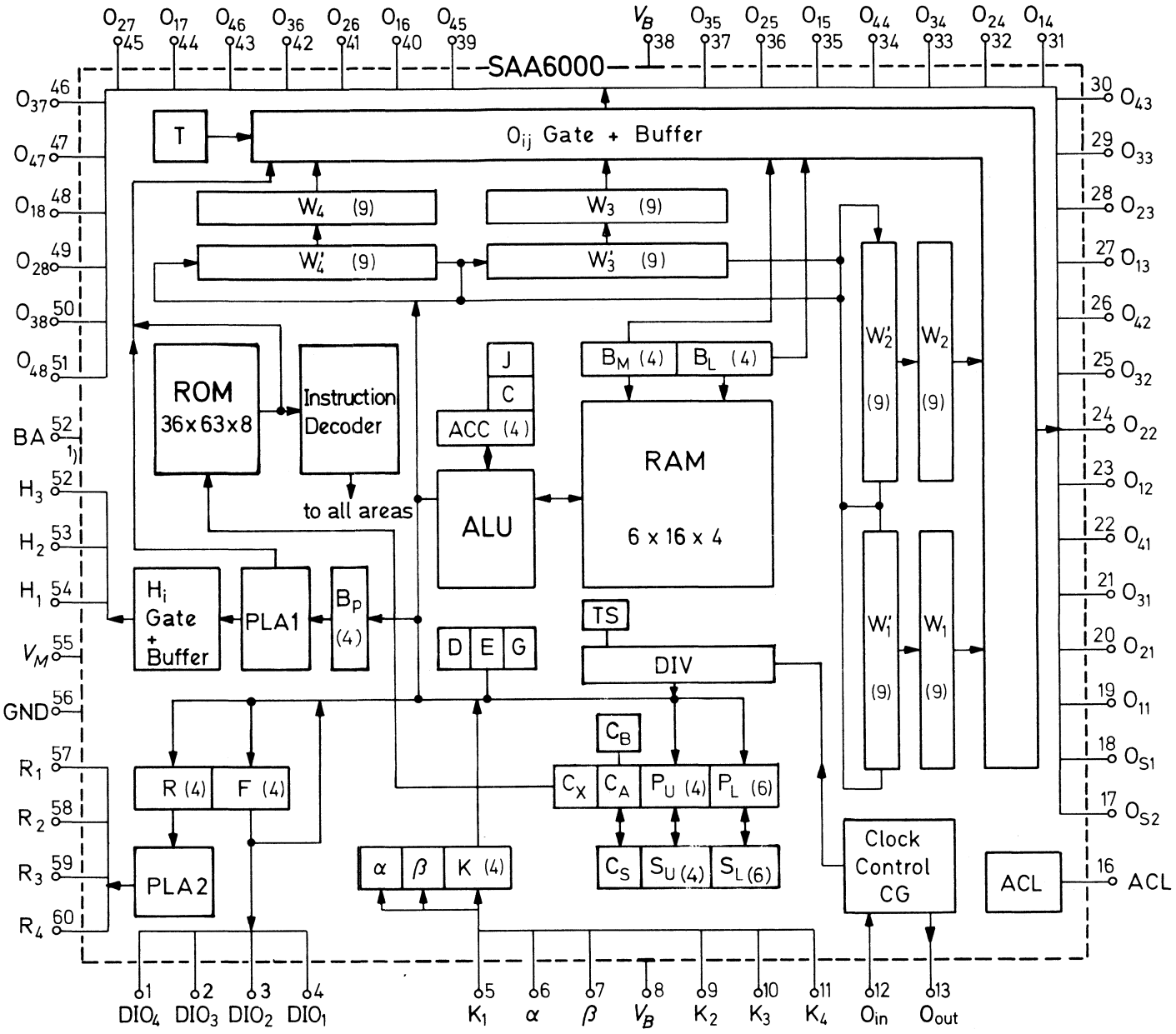


Fig. 2: Block diagram of the one-chip microcomputer SAA6000

2. Block Diagram

Pin Connections

$O_{11}...O_{48}$, O_{S1}, O_{S2}	Outputs
H_1 to H_3 [1])	Outputs, three-level
R_1 to R_4	Outputs
DIO_1 to DIO_4	Inputs/Outputs, tri-state
α and β	Asynchronous inputs
K_1 to K_4	Inputs
BA [1])	Input for low-voltage detection
O_{in}, O_{out}	Crystal oscillator terminals
GND	Ground, negative potential of supply voltage
V_B	Positive potential of supply voltage
V_M	Center tap of supply voltage
ACL	Switch-on initialisation

[1]) Because the number of terminals on the package is limited, either BA or H_3 is to be selected.

3. Electrical Parameters of the SAA6000

All voltages are referred to ground (GND).

Absolute Maximum Ratings

	Symbol	Value	Unit
Supply Voltages	V_B	−0.3 to +3.5	V
	V_M	−0.3 to +3.5	V
Ambient Operating Temperature Range	T_{amb}	−5 to +55	°C
Storage Temperature Range	T_S	−20 to +70	°C

Recommended Operating Conditions

	Symbol	Min.	Typ.	Max.	Unit
Supply Voltages	V_B	+2.6	–	+3.4	V
	V_M	0.45 V_B	0.5 V_B	0.55 V_B	V
Oscillator Frequency	f_{osc}		32768		Hz

Characteristics at V_B = +2.9 to +3.2 V, T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Current Consumption					
Standby Mode with LCD Clock Drive	$+I_D$	–	15	25	μA
in full Operation	$+I_D$	–	45	60	μA
Input Currents, Inputs ACL, α, β, DIO					
Low State (logic 0)	$-I_{IL}$	–	–	15	μA
High State (logic 1)	I_{HL}	–	–	15	μA
Input Voltages, Inputs K_1 to K_4, α, β					
Low State (logic 0)	V_{IL}	0	–	+0.6	V
High State (logic 1)	V_{IH}	V_B −0.6	–	V_B	V
Input Voltage, Input ACL					
Low State (logic 0)	V_{IL}	0	–	+0.3	V
High State (logic 1)	V_{IH}	V_B −0.3	–	V_B	V
Output Current, Outputs O_{11} to O_{48}, O_{S1}, O_{S2}, DIO_1 to DIO_4, R_2 to R_4	I_O	–	50	–	μA
Output R_1	I_O	–	100	–	μA
Voltage Drop Across the Output Transistors, Outputs O_{11} to O_{48}, O_{S1}, O_{S2}, DIO_1 to DIO_4, R_2 to R_4 at I_O = 50 μA	ΔV	–	–	0.5	V
Output R_1 at I_O = 100 μA	ΔV	–	–	0.2	V
Instruction Cycle for 1 byte Instructions	t_{i1b}	–	$\frac{2}{f_{osc}}$	–	s
Instruction Cycle for 2 byte Instructions	t_{i2b}	–	$\frac{4}{f_{osc}}$	–	s

4. Features of the telephone subset with SAA 6002

The SAA 6002 provides the following features:

- Quick-step dialling of an infinite number of digits (direct dialling)
- Selectable mark-space ratio and interdigital pause
- Access pause capability
- Repetition dialling; allows the repetition of the telephone number dialled last
- Repertory dialling capability; allows the repertory dialling of 10 telephone numbers with a maximum length of 16 digits each
- Single button dialling of four selectable emergency services with a maximum length of 16 digits each
- Elapsed time counter for minutes and seconds during a telephone call (stop watch)
- Counter for tariff pulses during a telephone call
- Direct drive of an 8-digit 7-segment LC display showing:
  Entered number
  Stored number
  Dialled number
  Present time (clock)
  Elapsed time of a call (stop watch)
  Number of tariff pulses of a call

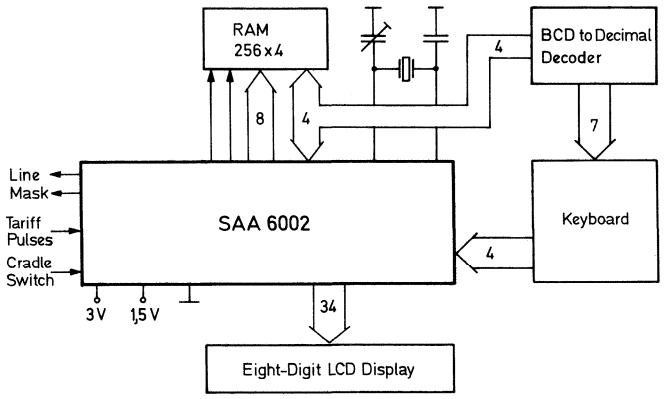


Fig. 3: Block diagram of a pushbutton telephone with SAA 6002

- 24 hour clock operation
- Key lock for blocking dialling except repertory dialling and emergency calls
- 3 V, 70 μA power supply

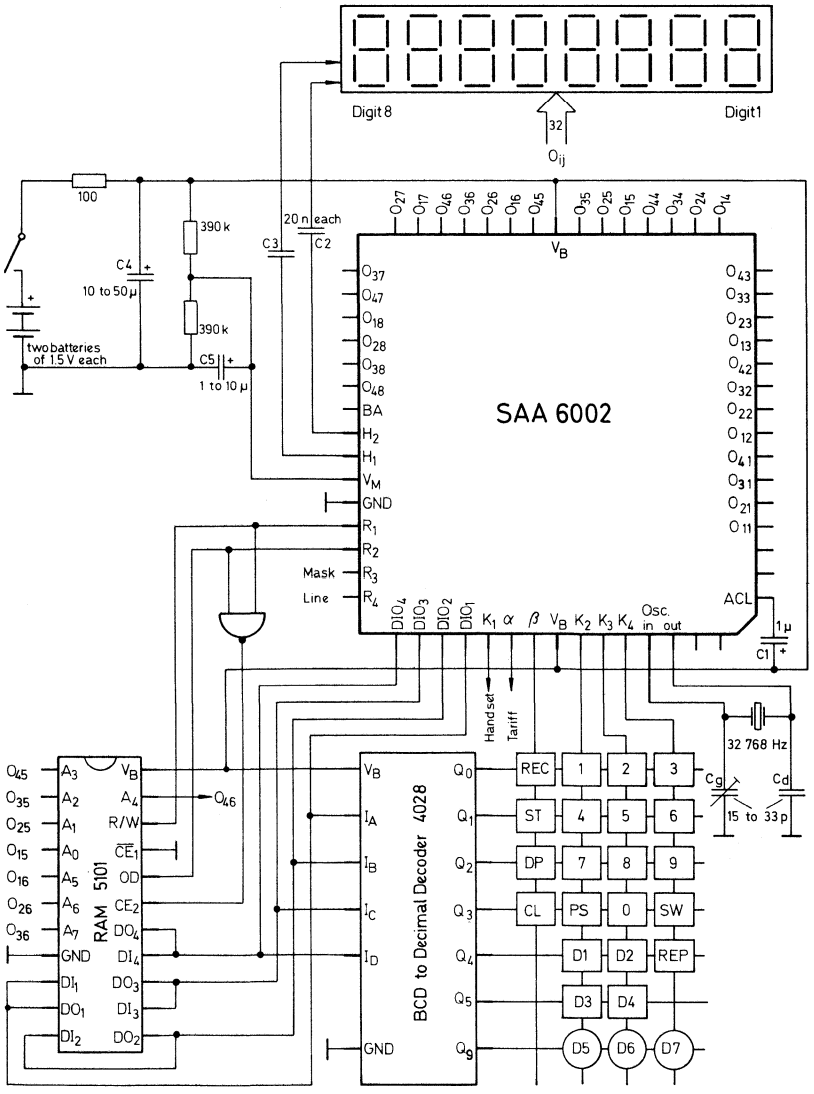


Fig. 4: System construction

5. Description of Functions

5.1. Power-on reset

As soon as power is supplied to the SAA6002, the program is reset. Depending on the state of the cradle switch (input K_1) the following actions are performed:

If the input K_1 is at L level, the display enters the clock display mode showing 0-00. Time counting is started and any key input is accepted.

If the input K_1 is at H level, the display is blanked and any key input of one of the digit keys 0 to 9 is accepted and dialling starts within 25 ms after power and clock are supplied.

5.2. Direct dialling

The display is immediately blanked when the K_1 input terminal (cradle switch input) becomes H level.

Desired telephone numbers can be keyed-in through the digit keys 0 to 9 and the PS key (ACCESS PAUSE key). The entered digits are displayed on the LC display, starting from the extreme right digit position, and they shift one by one to the left according to the new digit entries.

As a maximum of 8 digits is displayed, the first entered digit is shifted out from the display by the 9th digit entry. The display of these digit entries is active until the K_1 terminal becomes L level.

K_1 input	Key operation	Display	Remarks
H			blank
	0	0	starts dialling
	1	0 1	
	.	.	
	.	.	
	.	.	
	7	0 1 2 3 4 5 6 7	
	8	1 2 3 4 5 6 7 8	
↓ H	9	2 3 4 5 6 7 8 9	

As the numbers are keyed-in as shown above, the outputs are generated at R_4 (line output terminal) and R_3 (mask output terminal). The state of these outputs is shown in the Fig. 5. The generation of these outputs is continued as long as K_1 input is at H level.

As shown in Fig. 5, the mask output becomes active high after the end of bounce of the first keyed-in digit.

Acceptability of keyed-in digit numbers: no limitation.

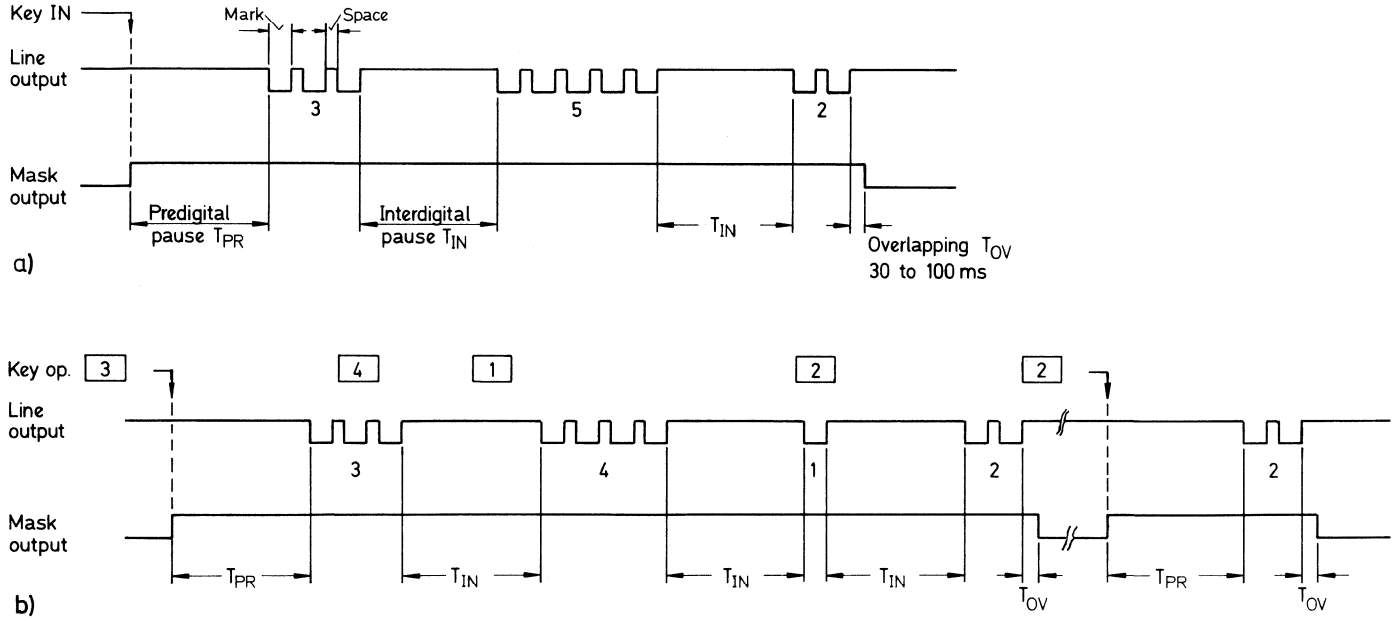


Fig. 5: Dialling pulse trains
a) auto dialling
b) direct dialling

5.3. Repetition dialling

The last dialled number is stored automatically, if a call was made by direct dialling and if this number has a maximum length of 16 digits, including access pauses. If the dialled number exceeds 16 digits, it is not stored.

The stored telephone number can be recalled and output can be generated as shown in the following example.

On the assumption that the number 07436-5-1321 is stored:

K_1 input	Key operation	Display	Remarks
H			blank
	REP	0 7 4 3 6 –	starts dialling
	REP	0 7 4 3 6 – 5 –	
↓ H	REP	6 – 5 – 1 3 2 1	

REP is the REPETITION key. As soon as the REP key is pressed, the SAA 6002 starts generating the output. The display starts with the extreme right digit and the number shifts to the left and stops when an access pause appears. In the example above, the display starts from 0 and shifts one by one to the left, generating the output and stops when an access pause appears after 6; then also the output stops.

When the REP key is pressed again, the SAA 6002 generates the output, shifts the display and stops the output and the display shifting at the next access pause. Furthermore, when the REP key is pressed once more, the SAA 6002 generates the output again until the last digit (i.e. 1) appears.

If the REP key is pressed while the display is shifted, the SAA 6002 stops generating the output and the display is blanked. The stored contents of the telephone number dialled last remain unchanged. Another actuation of the REP key (K_1 still being at H level) starts generating the output from the beginning of this telephone number.

Making K_1 input L level during repetition dialling cancels the call and the display returns to the real time clock display mode. The stored contents remain unchanged.

5.4. Repertory dialling

Repertory dialling allows to store up to 10 telephone numbers with a maximum length of 16 digits each, including access pauses, for automatic dialling.

5.4.1. To store a number for repertory dialling

Example: Store 07436-5-1321 into memory location 2.

ST is the STORE key. As soon as the ST key is released, the entered telephone number is stored and the display shows the present time.

K_1 input	Key operation	Display	Remarks
L	ST		blank
	2		blank
	0	0	
	7	0 7	
	4	0 7 4	
	3	0 7 4 3	
	6	0 7 4 3 6	
	PS	0 7 4 3 6 –	
	5	0 7 4 3 6 – 5	
	PS	0 7 4 3 6 – 5 –	
	1	7 4 3 6 – 5 – 1	
	3	4 3 6 – 5 – 1 3	
	2	3 6 – 5 – 1 3 2	
	1	6 – 5 – 1 3 2 1	
	ST	6 – 5 – 1 3 2 1	finish
↓ L		1 2 – 3 4	present time

5.4.2. To recall a number for repertory dialling

Example: To recall a number and to generate the output on the assumption that the number 07436-5-1321 is stored at memory location 2.

K_1 input	Key operation	Display	Remarks
H			blank
	REC		blank
	2	0 7 4 3 6 –	starts dialling
	REP	0 7 4 3 6 – 5 –	
↓ H	REP	6 – 5 – 1 3 2 1	

REC is the RECALL key. With the depression of the 2 key, the SAA 6002 starts generating the output indicating the first digit 0 at the extreme right position. Then, the SAA 6002 shifts the stored number one by one to the left and stops when an access pause appears. Further key operation and sequence is identical as described in paragraph 5.3.

If the REP key is pressed while the display is shifted, the dialler stops generating the output.

5.5. Emergency services

Single button dialling enables four selectable emergency calls with a max. length of 16 digits each to be dialled.

5.5.1. To store a number for emergency calls

Example: To store the number 04541-3476 into memory location D2.

K_1 input	Key operation	Display	Remarks
L	ST		blank
	D2		blank
	0	0	
	4	0 4	
	5	0 4 5	
	4	0 4 5 4	
	1	0 4 5 4 1	
	PS	0 4 5 4 1 –	
	3	0 4 5 4 1 – 3	
	4	0 4 5 4 1 – 3 4	
	7	4 5 4 1 – 3 4 7	
	6	5 4 1 – 3 4 7 6	
	ST	5 4 1 – 3 4 7 6	finish
L		1 2 – 3 4	present time

As soon as the ST key is released, the entered telephone number is stored and the display shows the present time.

5.5.2. To recall an emergency number

Example: To recall an emergency number on the assumption that 04541-3476 is stored at memory location D2.

K_1 input	Key operation	Display	Remarks
H			blank
	D 2	0 4 5 4 1 –	starts dialling
H	REP	5 4 1 – 3 4 7 6	

If the REP key is pressed while the display is shifted, the dialler stops generating the output.

5.6. Display of stored numbers

Stored numbers can be recalled by the following key operations. The K_1 input is kept at L level during recalling.

5.6.1. Display of stored repetition dialling numbers

Example: Supposing that the telephone number dialled last is 07436-5-1321.

K_1 input	Key operation	Display	Remarks
L	DP		blank
	REP	0 7 4 3	
	DP	6 – 5 – 1 3 2 1	
L		1 2 – 4 3	present time

DP is the DISPLAY key. The DP key is pressed constantly during recalling.

The first digits are displayed as long as the REP key is pressed. Releasing this key, the last 8 digits are displayed.

Releasing the DP key, the display returns to show the present time.

5.6.2. Display of stored repertory dialling numbers

Example: Supposing that the number 0123-45678-910 is stored at memory location 0.

K_1 input	Key operation	Display	Remarks
L	DP		blank
	0	0 1 2 3 – 4	
	DP	5 6 7 8 – 9 1 0	
L		1 2 – 3 4	present time

The DP key is pressed constantly during recalling.
The first digits are displayed during the depression of the 0 key.
Releasing this key, the last 8 digits are displayed.
Releasing the DP key, the display returns to show the present time.

5.6.3. Display of stored emergency call numbers

Example: Supposing that the number 04541-3476 is stored at memory location D2.

K_1 input	Key operation	Display	Remarks
L	DP		blank
	D2	0 4	
	DP	5 4 1 – 3 4 7 6	
L		1 2 – 3 4	present time

The DP key is pressed constantly during recalling.
The first digits are displayed during the depression of the D2 key. Releasing this key, the last 8 digits are displayed.
Releasing the DP key, the display returns to show the present time.

5.7. Clock

With the K_1 input at L level, the display normally shows the present time in the 24 hours display format: hours at the first 2 digits from the left, minutes at the 4th and 5th digit from the left. Hours and minutes are separated by a dash (at the 3rd digit from the left).

5.7.1. Time setting

Time setting can be accomplished as shown in the following example: To set the time to 12 : 34.

K_1 input	Key operation	Display	Remarks
L	CL	–	
	1	1 –	
	2	1 2 –	
	3	1 2 – 3	
	4	1 2 – 3 4	
	CL	1 2 – 3 4	
L		1 2 – 3 4	finish: sec. starts from 0 0

CL is the CLOCK key.

5.8. Stop watch

With the K_1 input at H level (i.e. off-hook state), stop watch can be operated. The elapsed time of a call can be displayed with minutes and seconds separated by a dash: minutes at the 4th and 5th digit from the right, seconds at the 1 st and 2 nd digit from the right. The stop watch starts counting from 00-00 and counts up to 99-59 (99 min and 59 sec).

An example of operation flow is shown in the following.

K_1 input	Key operation	Display	Remarks
L		1 2 – 3 5	clock mode (real time)
H			blank
		min sec	
	SW	0 0 – 0 0	stop watch mode, starts counting
		min sec	
		0 0 – 0 1	
		.	
		.	
		.	
		min sec	
H		9 9 – 3 0	
		hour min	
L		1 4 – 1 5	clock mode

SW is the STOP WATCH key. Pressing the SW key after lifting the handset (i.e. K_1 input is at H level) enables the stop watch to start counting, erasing the old information. However, SW key operation is ignored while generating the line output.

The stop watch stops counting by replacing the handset (i.e. K_1 input becomes L level) whereby the display returns to show the present time. The counted values are memorized and can be recalled afterwards.

5.8.1. To recall the elapsed time and tariff pulses of the last call

After a telephone call, the counted values can be recalled sequentially with the SW key. The state of the K_1 input does not matter.

Key operation	Display	Remarks
SW	1 2 – 3 4	clock mode
SW	1 5 7	tariff pulse mode
SW	0 1 – 3 7	stop watch mode

Pressing the SW key while the K_1 input is at H level activates the stop watch mode and starts counting. Presssing the SW key once more causes the display to return to the clock display mode keeping the stop watch counting (see above flow). With the next actuation of the SW key the tariff pulses are displayed. When the K_1 input becomes L, the display always returns to clock mode.

5.9. Display of tariff pulses

If the K_1 input becomes H, the tariff pulse counter is reset and then counts up pulses supplied to the α input.

If the K_1 input becomes L, the counted number of tariff pulses are stored and the display returns to the clock mode. Stored number of tariff pulses during a call can be recalled. Refer to paragraph 5.8.1.

Max. countable numbers : 0 to 999.

Tariff pulses are not accepted while generating the line output.

5.10. Determination of operation mode

The operation mode can be determined as follows by constructing a matrix at the keyboard section, see Fig. 6.

5.10.1. Mark-space ratio

D5 not existing : mark-space = 2 : 1
D5 connected : mark-space = 1.6 : 1
Mark + space = 100 ms

5.10.2. Interdigital pause and predigital pause

D6 not existing : 925 ms
D6 connected : 425 ms
Interdigital pause and predigital pause are of the same length.

5.10.3. Key lock

D7 not existing : no blocking
D7 connected : blocks dialling except repertory dialling and emergency calls.

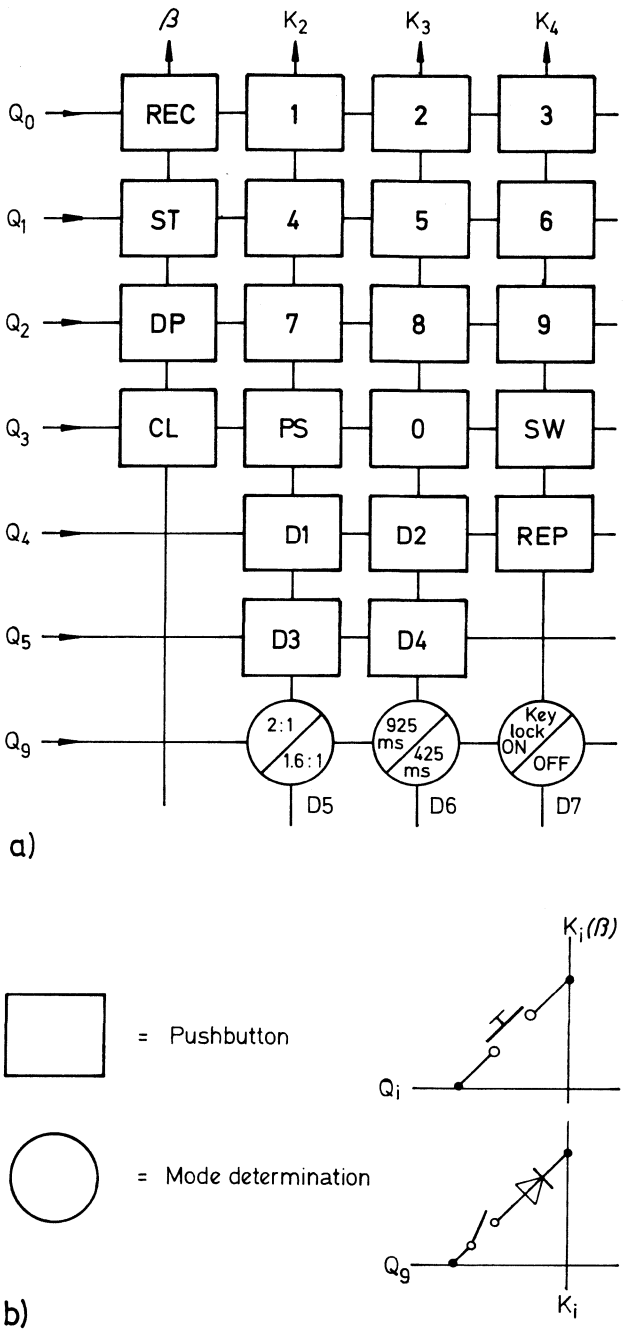


Fig. 6: Keyboard
a) arrangement
b) contacts

6. LCD drive

The 8-digit 2 phase multiplexed LCD is driven directly by the SAA6002. The LCD partitioning is shown in Fig. 7, the LCD pattern in Fig. 8. The threshold voltage of the LCD has to be chosen such that the LCD is switched off when a signal with an amplitude of ±1.5 V is applied, and switched on when the amplitude is ±3 V.

Digit	H_1	H_2	Segment signal output terminals O_{ij}
8	c8	d8	O_{11}
	g8	e8	O_{21}
	a8	f8	O_{31}
	b8		O_{41}
7	c7	d7	O_{12}
	g7	e7	O_{22}
	a7	f7	O_{32}
	b7		O_{42}
6	c6	d6	O_{13}
	g6	e6	O_{23}
	a6	f6	O_{33}
	b6		O_{43}
5	c5	d5	O_{14}
	g5	e5	O_{24}
	a5	f5	O_{34}
	b5		O_{44}
4	c4	d4	O_{15}
	g4	e4	O_{25}
	a4	f4	O_{35}
	b4		O_{45}
3	c3	d3	O_{16}
	g3	e3	O_{26}
	a3	f3	O_{36}
	b3		O_{46}
2	c2	d2	O_{17}
	g2	e2	O_{27}
	a2	f2	O_{37}
	b2		O_{47}
1	c1	d1	O_{18}
	g1	e1	O_{28}
	a1	f1	O_{38}
	b1		O_{48}

Fig. 7: LCD partitioning

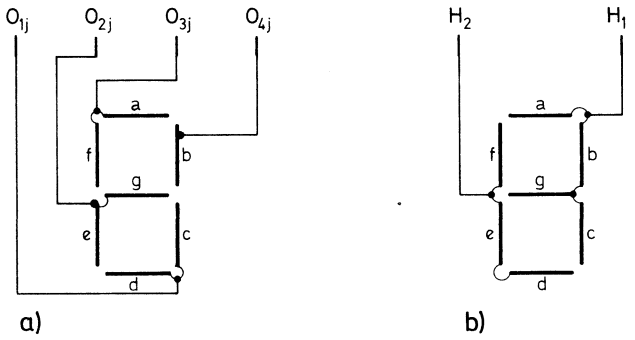


Fig. 8: LCD pattern
a) segment side
b) common side

Dual-Tone Multi-Frequency Telephone Dialer

Features

- Minimum external parts count
- High-accuracy tones
- Digital divider logic, resistive ladder network and CMOS operational amplifier on single chip
- Uses inexpensive 3.579545 MHz television color-burst crystal
- Invalid key entry can result in either single tone or no tone
- Tone Disable allows Any Key Down output to function from keyboard input without generating tones

Description

The SBA5089 is a monolithic integrated CMOS circuit. It uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone Multi-Frequency (DTMF) telephone dialing.

The SBA5089 was designed specifically for integrated tone-dialer applications that require the following: fixed supply operation, negative-true keyboard-input, $\overline{\text{Tone Disable}}$ input, stable-output tone level, and an Any Key Down output that is open circuit when no keyboard buttons are pushed and pulls to GND when a button is pushed.

Keyboard entries cause the selection of the proper divide ratio to obtain the required two audio frequencies from the 3.579545 MHz reference oscillator. D-to-A conversion is accomplished on-chip by a conventional R-2R ladder network. The tone output is a stairstep approximation to a sinewave and requires little filtering for low-distortion applications. The same operational amplifier that accomplishes the current-to-voltage transformation necessary for the D-to-A converter also mixes the low and high group signals. Frequency-stability of this type of tone generation is such that no frequency adjustment is needed to meet standard DTMF specifications.

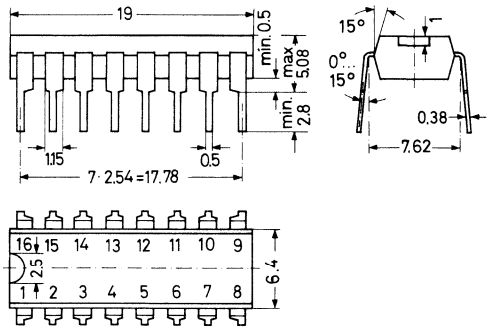


Fig. 2:
SBA5089 in 16-pin plastic package 20 A 16 according to DIN 41866

Weight approximately 1.2 g
Dimensions in mm

Pin Connections

1 $\overline{\text{Supply Voltage}}$ V_B
2 $\overline{\text{Tone Disable}}$ Input
3 Column Input C_1
4 Column Input C_2
5 Column Input C_3
6 Ground, GND
7 Oscillator Input Osc.in
8 Oscillator Output Osc.out
9 Column Input C_4
10 Any Key Down Output AKD
11 Row Input R_4
12 Row Input R_3
13 Row Input R_2
14 $\overline{\text{Row Input}}$ R_1
15 $\overline{\text{Single Tone Inhibit}}$ Input
16 Tone Output

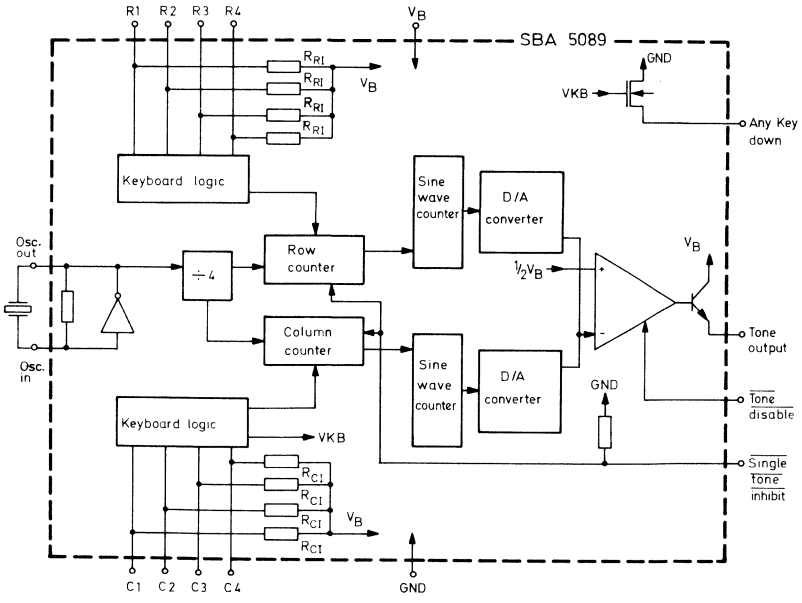


Fig. 1:
SBA5089 block diagram

Absolute Maximum Ratings

	Symbol	Value	Unit	Conditions
Supply Voltage	V_B	10.5	V	
Any Input relative to V_B (except pin 10)	V_n	0.3	V	
Any Input relative to GND (except pin 10)	V_n	−0.3	V	
Ambient Operating Temperature Range	T_A	−30 to +60	°C	
Storage Temperature Range	T_S	−55 to +150	°C	
Maximum Circuit Power Dissipation	P_{tot}	500	mW	see Fig. 3

Operating Characteristics at $-30\ °C \leq T_A \leq 60\ °C$

	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_B	3	–	10	V	
Input "0"	V_{IL}	0	–	0.3 V_B	V	
Input "1"	V_{IH}	0.7 V_B	–	V_B	V	
Input Pull-Up Resistor	R_I	20	–	100	kΩ	
$\overline{\text{Tone Disable}}$	$\overline{TD}$	0	–	0.3 V_B	V	see Note 4
Tone Output	V_{out}	−10	–	−7	dBm	see Note 1
Pre Emphasis, High Band	–	2.4	2.7	3	dB	
Output Distortion, measured in terms of total out-of-band power relative to RMS sum of Row and Column fundamental power	–	–	–	−20	dB	see Note 2
Rise Time	T_{rise}	–	2.8	5	ms	see Note 3
Any Key Down Sink Current to GND	I_{AKD}	500	–	–	μA	at V_{out} = 0.5 V
AKD Off Leakage Current	I_{AKDO}	–	–	2	μA	at V_{out} = 5 V
Supply Current Operating	I_{SO}	–	–	2	mA	at V_B = 3.5 V see Note 6
Supply Current Standby	I_{SST}	–	–	200	μA	at V_B = 10 V see Note 5
Tone Output – No Key Down	NKD	–	–	−80	dBm	

Notes

1: Single-tone, low-group. Any V_B between 3.4 V and 3.6 V, 0 dBm = 0.775 V, R_{LOAD} = 100 kΩ. See Test Circuit Fig. 9.

2: Any dual-tone. Any V_B between 3.4 V to 10.0 V.

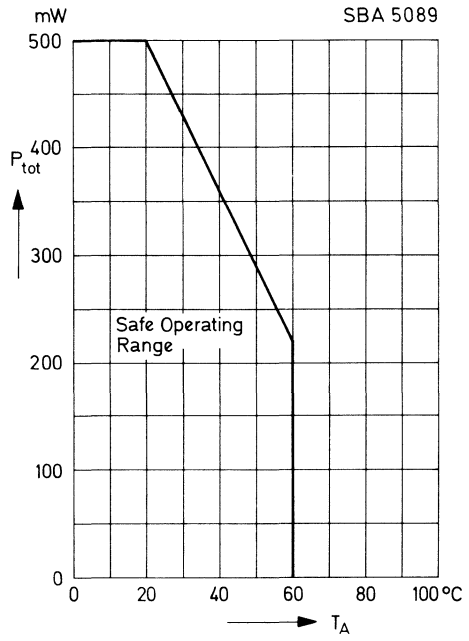
3: Time from a valid keystroke with no bounce to allow the waveform to go from min. to 90% of the final magnitude of either frequency.
Crystal parameters defined as R_S = 100 Ω, L = 96 mH, C = 0.02 pF, and C_h = 5 pF. $V_B \geq 3.4$ V. f = 3.579545 MHz.

4: Only tones will be disabled when $\overline{TD}$ is taken to logical "0". Other chip functions may activate. Pull-up resistor on $\overline{TD}$ input will meet same spec. as other inputs. Logic 0 = GND.

5: Stand-by condition is defined as no keys activated, $\overline{TD}$ = Logical 1, Single $\overline{\text{Tone Disable}}$ = Logical 0.

6: One key depressed only. Outputs unloaded.

Fig. 3:
Admissible power dissipation versus temperature



Oscillator

The network contains an on-board inverter with sufficient loop gain to provide oscillation when used with a low cost television color-burst crystal. The inverter's input is Osc.in (pin 7) and output is Osc.out (pin 8). The circuit is designed to work with a crystal cut to 3.579545 MHz to give the frequencies in Table 1.

Table 1:
Standard DTMF and output frequencies of the SBA5089

	Standard DTMF	Tone Output Frequency using 3.579545 MHz Crystal	Deviation from Standard
	Hz	Hz	%
f_1	697	701.3	+0.62
f_2	770	771.4	+0.19
f_3	852	857.2	+0.61
f_4	941	935.1	− 0.63
f_5	1209	1215.9	+0.57
f_6	1336	1331.7	− 0.32
f_7	1477	1471.9	− 0.35
f_8	1633	1645.0	+0.73

Any crystal frequency deviation from 3.579545 MHz will be reflected in the tone output frequency. Most crystals don't vary more than 0.02%.

Output Tone Levels

The output tone level of the SBA5089 is proportional to the applied DC supply voltage. Operation will normally be with a regulated supply. This results in enhanced temperature stability, since the supply voltage may be made temperature stable.

Keyboard Configuration

Each keyboard input is standard CMOS with a pull-up resistor to V_B. These inputs may be controlled by a keyboard or electronic means. Open collector TTL or standard CMOS (operated off same supply as the SBA5089) may be used for electronic control. The switch contacts used in the keyboards may be void of precious metals, due to the CMOS network's ability to recognize resistance up to 1 kΩ as a valid key closure.

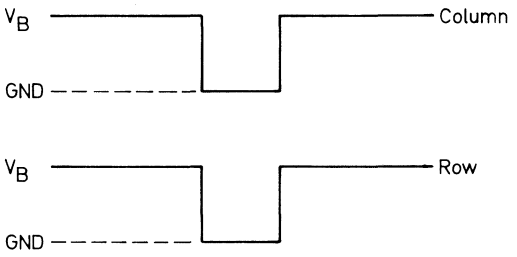


Fig. 4:
Electronic input pulses

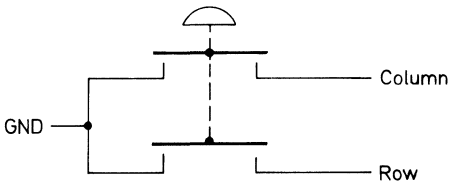


Fig. 5:
2 of 8 DTMF keyboard

Row and Column Inputs

With Single Tone Inhibit at V_B, connection of GND to a single column will cause the generation of that column tone. Connection of GND to more than one column will result in no tones being generated. The application of GND to only a row pin or pins has no effect on the circuit. There must always be at least one column connected to GND for row tones to be generated. If a single row tone is desired, it may be generated by tying any two column pins and the desired row pin to GND. Dual tones will be generated if a single row pin and a single column pin are connected to GND.

Any Key Down Output (Pin 10)

The Any Key Down output is used for electronic control of receiver and/or transmitter switching and other desired functions. It switches to GND when a keyboard button is pushed, and is open circuited when not. The AKD output switches regardless of the Tone Disable and Single Tone Inhibit inputs.

$\overline{\text{Tone}}$ $\overline{\text{Disable}}$ Input (Pin 2)

The $\overline{\text{Tone}}$ $\overline{\text{Disable}}$ input is used to defeat tone generation when the keyboard is used for other functions besides DTMF signaling. It has a pull-up to V_B and when tied to GND tones are inhibited. All other chip functions operate normally.

$\overline{\text{Single}}$ $\overline{\text{Tone}}$ Inhibit Input (Pin 15)

The Single Tone Inhibit input is used to inhibit the generation of other than dual tones. It has a pull-down to GND and when floating or tied to GND, any input situation that would normally result in a single tone will now result in no tone, with all other chip functions operating normally.

When forced to V_B, single or dual tones may be generated as described in the paragraph under Row and Column Inputs.

Output Waveform

The row column output waveforms are shown in Figure 6. These waveforms are digitally synthesized using on-chip D-to-A converters. Distortion measurement of these unfiltered waveforms will show a typical distortion of 7% or less. The on-chip operational amplifier of the SBA5089 mixes the row and column tones together to result in a dual-tone waveform. Special analysis of this waveform will show that typically all harmonic and intermodulation distortion components will be –30 dB down when referenced to the strongest fundamental (column tone). Figures 7 and 8 show a typical dual tone waveform and its spectral analysis.

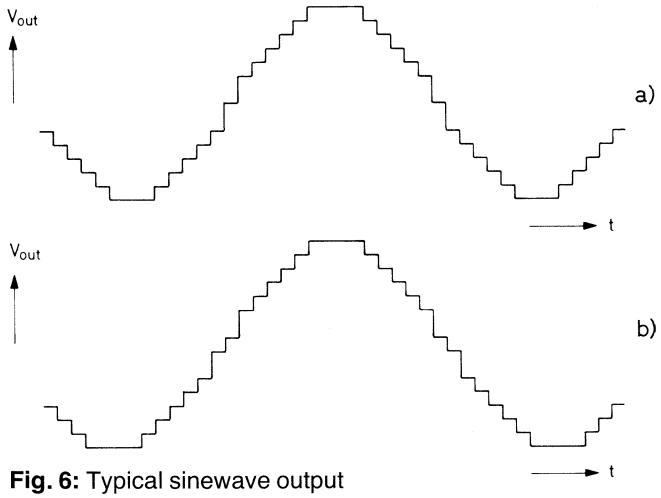


Fig. 6: Typical sinewave output
a) Row tones b) Column tones

Tone Output (Pin 16)

The Tone Output pin is connected internally in the SBA5089 to the emitter of an NPN transistor whose collector is tied to V_B. The input to this transistor is the on-chip operational amplifier which mixes the row and column tones together and provides output level regulation.

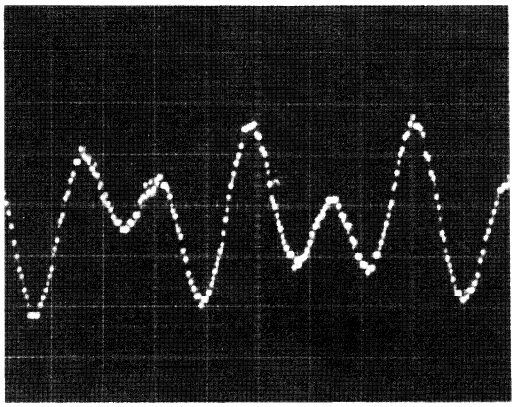


Fig. 7:
Typical dual tone waveform (Row 1, Column 1)

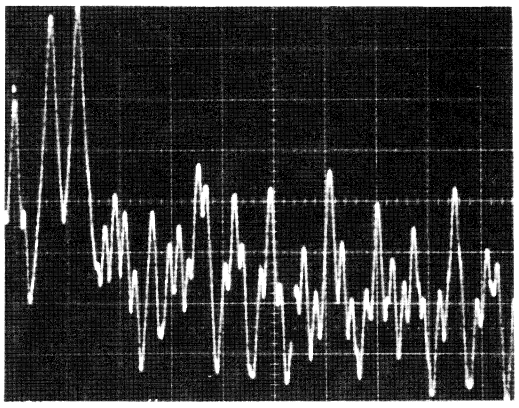


Fig. 8:
Spectral analysis of waveform in Fig. 7
(Vert.: 10 dB/Div., Horizontal: 1 kHz/Div.)

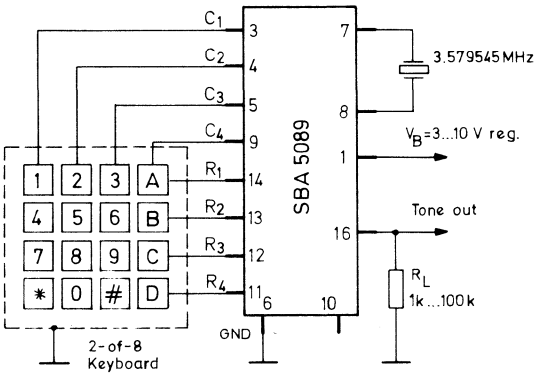


Fig. 9:
Tone output test circuit
Note: 1 kΩ < R_{LOAD} < 100 kΩ

SBA5091

Dual-Tone Multi-Frequency Telephone Dialer

Features

- CEPT compatible
- High-accuracy tones
- Digital divider logic, resistive ladder network, CMOS operational amplifier, and bipolar driver on chip
- Uses inexpensive 3.579545 MHz television color-burst crystal
- Invalid key entry can result in either single tone or no tone
- Designed for use with calcutator type (class A contact) keyboards or 2-of-8 keyboards
- Low standby power for continuous on-line operation

Description

The SBA5091 is an monolithic integrated CMOS circuit and is designed specifically to meet European CEPT specifications. It uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone Multi-Frequency (DTMF) telephone dialing.

The keyboard entries select the proper digital dividers to divide the 3.579545 MHz to obtain the unique audio frequencies required. The digital signals are then processed by a R-2R ladder network, and current-to-voltage transformation is made by an on-chip amplifier. This is a conventional D-to-A converter and yields sine waves of sufficient purity that filtering is easily accomplished. The same amplifier accomplishes summing of the low-and-high group tones to obtain the required dual-tone signal. Frequency accuracy of the network is obtained via the crystal reference which eliminates any need for frequency adjustment.

The SBA5091 meets the following integrated tone dialer application requirements: compatibility with European CEPT specifications, regulated-supply operation, single contact keyboard input, Chip-Disable input, stable output tone level, and an Any Key Down output that is open circuit when no keyboard buttons are pushed, and pulls to V_B when a button is pushed.

Supplied in an 18-pin plastic package, the SBA5091 provides two pins for tone filtering of the multiple stairstep output sine wave. Typically, only three resistors and two capacitors are needed to produce sine waves of sufficient purity to meet the CEPT harmonic distortion specification.

The SBA5091 high-group pre-emphasis before filtering is typically 2.0 dB. Output level meets European applications.

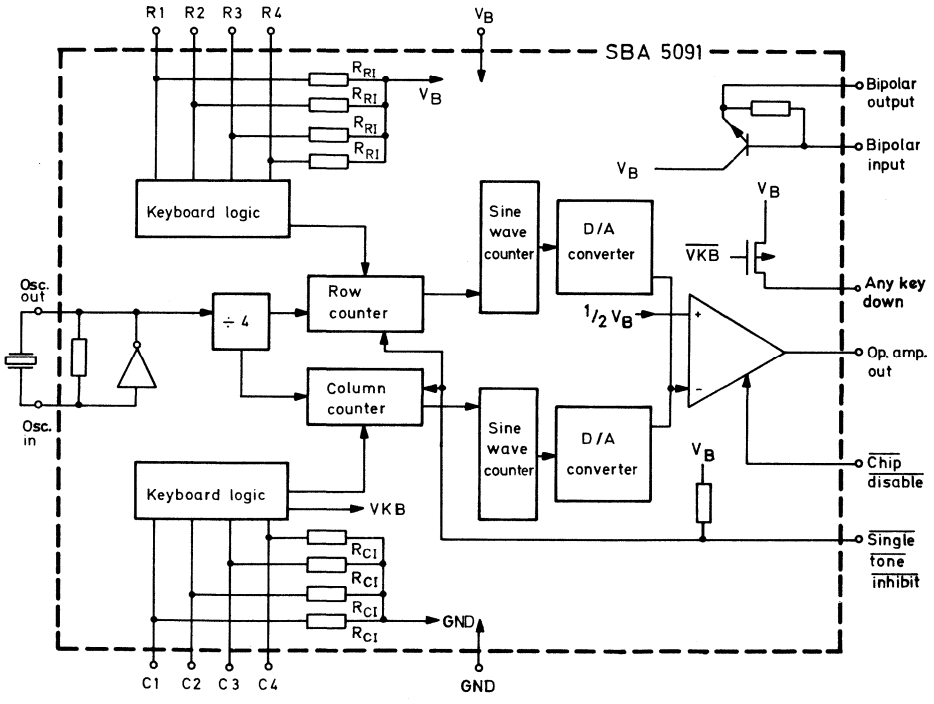


Fig. 1:
SBA5091 block diagram

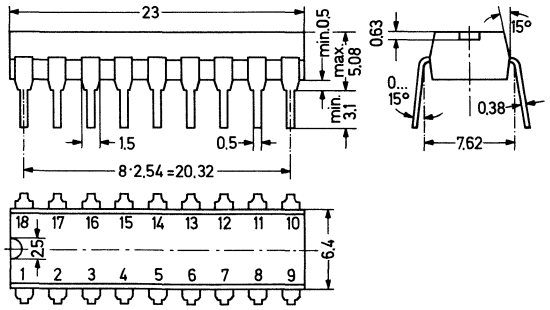
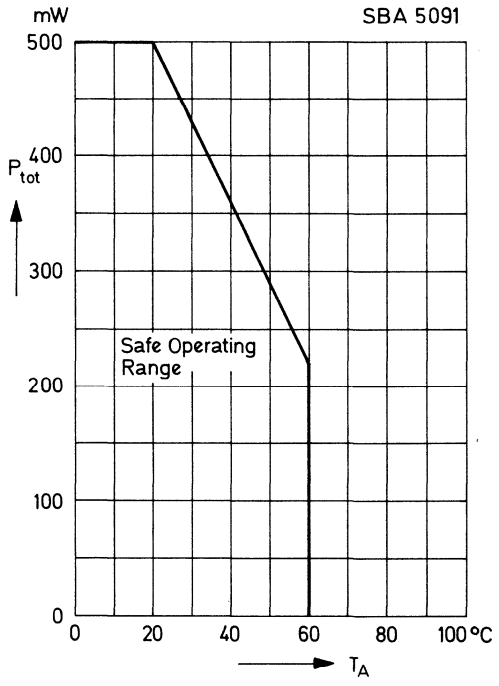


Fig. 2:
SBA5091 in 18-pin plastic package 20 A 18 according to DIN 41866

Weight approximately 1.5 g
Dimensions in mm

Fig. 3:
Admissible power dissipation versus temperature



Pin Connections

1	Op Amp Output	9	Oscillator Output Osc.out
2	Supply Voltage V_B	10	Column input C_4
3	Chip Disable Input CD	11	Any Key Down Output AKD
4	Column Input C_1	12	Row Input R_4
5	Column Input C_2	13	Row Input R_3
6	Column Input C_3	14	Row Input R_2
7	Ground, GND	15	Row Input R_1
8	Oscillator Input Osc.in	16	Single Tone Inhibit Input STI
		17	Bipolar Input

Absolute Maximum Ratings

	Symbol	Value	Unit	Conditions
Supply Voltage	V_B	10.5	V	
Voltage on any Pin relative to V_B	V_n	0.3	V	
Voltage on any Pin relative to GND	V_n	−0.3	V	
Ambient Operating Temperature Range	T_A	−30 to +60	°C	
Storage Temperature Range	T_S	−55 to −150	°C	
Maximum Circuit Power Dissipation	P_{tot}	500	mW	see Fig. 3

Operating Characteristics at –30 °C ≤ T_A ≤ +60 °C; all voltages referenced to GND = 0.0 V

	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage						
Operating (Generating Tones)	V_B	3.0		10.0	V	
Standby (DC Switching Only)	V_B	2.0		10.0	V	1
Inputs						
$\overline{\text{Chip Disable}}$, $\overline{\text{Single Tone Inhibit}}$						
Input High (Logic 1)	V_{IH}	0.7 V_B		V_B	V	
Input Low (Logic 0)	V_{IL}	0.0		0.3 V	V	
Colums (1 to 4)						
Input High (Column ON)		0.7 V_B		V_B	V	
Input Low (Column OFF)		0.0		+0.30	V	
Row (1 to 4)						
Input High (Row OFF)		V_B –0.30		V_B	V	
Input Low (Row ON)		0.0		0.3 V_B	V	
Input Resistance (CD and STI only)	R_I	20		100	kΩ	10
Tone Output Level, Pin 1	V_{out}	–10.0	–8.5	–7.0	dBm	2, 11
Pre-Emphasis, Highband (Unfiltered)		1.0	2.0	3.0	dB	3, 11
Output distortion measured in terms of out of band power relative to RMS sum of row and column fundamental power				–20	dB	4, 11
Rise Time	t_r			5	ms	5
Any Key Down Source Current to V_B	$I_{AKD_{ON}}$	500			μA	6
Any Key Down Off Leakage	$I_{AKD_{OFF}}$			10	μA	7
Supply Current, Operating						
at 3.5 V	I_{OP}		1.0	2.0	mA	8
at 10.0 V			5.0		mA	
Supply Current, Standby at 10.0 V	I_{SB}		1.0	200	μA	9
Tone Output, No Key Down				–80	dBm	
Op Amp Output Resistor			10		KΩ	12
Op Amp Output Current at 3.0 V		250			μA	12

Notes

1: Voltage at which Any Key Down output will respond to any key closure, Chip Disable = 0.
2: Single tone, low group. Any supply voltage between 3.4 V and 3.6 V. Output amplitude is linearly proportional to supply voltage. This condition valid for –30 °C < T_A < 60 °C. See test circuit, Fig. 4.
3: High-group output level relative to low-group level. Valid for –30 °C < T_A < 60 °C.
4: Any supply voltage between 3.4 V and 10.0 V. See test circuit, Fig. 4.
5: Time from a valid keystroke with no bounce to allow the output waveform to go from its minimum to 90% of the final magnitude of either frequency. Crystal parameters are defined to be R_S = 100 Ω, Lm = 96 mH, CM = 0.02 pF, and Ch = 5 pF. F = 3.579545 MHz. Any –30 °C <T_A < +60 °C.
6: AKD is open drain P-channel transistor. Minimum current defined is valid with V_B = 3.5 volts, V_{AKD} = 3.0 volts. AKD pulls to V_B when valid key is depressed.
7: V_B = 10 V, V_{AKD} = 0 V.
8: For any ambient temperature in the range –30 °C to +60 °C. Single key depressed only. Crystal as in Note 5. Measured at Pin 6.
9: Standby condition is defined to be no keys activated, CD = logical 0, Single Tone Inhibit = logical 1.
10: 25 °C.
11: R_L (pin 18) = 620 Ω at 3.4 V ≤ V_B ≤ 5 V. See test circuit, Fig. 4.
330 Ω at V_B > 7.5 V.
12: Op Amp Output Resistor size is determined by the capacitance on Pin 1. The 10 KΩ resistor shown in test circuit Fig. 4 is correct for typical filter circuit. If capacitance at this pin is too large, a smaller value of resistance will be required.

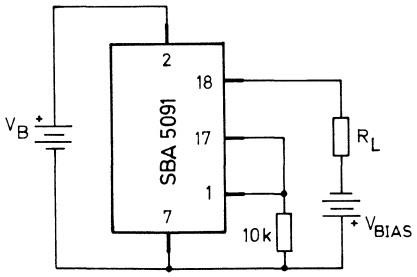


Fig. 4:
Test circuit
V_{BIAS} = 0.5 V when $V_B \leq 4.0$ V
V_{BIAS} = 0 V when $V_B > 4.0$ V

Output Tone Levels

The output tone level of the SBA5091 is proportional to the applied DC supply voltage. Operation will normally be with a regulated supply. This results in enhanced temperature stability, since the supply voltage may be made temperature stable.

Distortion

The dual-tone harmonic requirement of the European CEPT specification is as follows:

The level of any individual unwanted frequency component relative to the fundamental of the low group shall not exceed the following limits (0 dBm = 0.775 Volts):

In the freq. band 300 to 3400 Hz: 33 dBm.

In the freq. band 3.4 to 50 KHz: 33 dBm at 3.4 KHz, falling at 12 dB per octave to 50 KHz.

In the freq. band above 50 KHz: 80 dBm.

A two-pole filter is required to fulfill the above distortion requirements. This filter may be constructed using the bipolar transistor available at pins 17 and 18 of the SBA5091. The two poles should be placed at approximately 3.4 KHz. Additional margin may be obtained by reducing the frequency of these poles, but a practical limit is reached when the amount of preemphasis becomes altered.

$\overline{\text{Chip}}$ $\overline{\text{Disable}}$ (Pin 3)

The Chip Disable input is used to defeat tone generation when the keyboard is used for other functions besides DTMF signaling. This input has a pull up to V_B supply during keyboard entry and when left floating or tied to V_B, tones are generated normally. When forced to GND, tones are inhibited. All other chip functions operate normally.

Any Key Down (Pin 11)

The Any Key Down output is used for electronic control of receiver and/or transmitter switching and other desired functions. It switches to V_B when a keyboard button is pushed, and is open-circuited when not. The AKD output switches regardless of the $\overline{\text{Chip}}$ $\overline{\text{Disable}}$ and $\overline{\text{Single}}$ $\overline{\text{Tone}}$ $\overline{\text{Inhibit}}$ inputs.

$\overline{\text{Single}}$ $\overline{\text{Tone}}$ $\overline{\text{Inhibit}}$ (Pin 16)

The $\overline{\text{Single}}$ $\overline{\text{Tone}}$ $\overline{\text{Inhibit}}$ input is used to inhibit the generation of other than dual tones. It has a pull up to V_B, and when left floating or tied to V_B, single or dual tones may be generated as described in the paragraph under row-column inputs. When forced to GND, any input situation that would normally result in a single tone will now result in no tone, with all other chip functions operating normally.

Oscillator

The network contains an on-board inverter with sufficient loop-gain to provide oscillation when working with a low-cost television color-burst crystal. The inverter's input is Osc. in (pin 8) and output is Osc. out (pin 9). The circuit is designed to work with a crystal cut to 3.579545 MHz to give the frequencies in Table 1.

Table 1:
Standard DTMF and output frequencies of the SBA5091

	Standard DTMF Hz	Tone Output Frequency using 3.579545 MHz Crystal Hz	Deviation from Standard %
f_1	697	701.3	+0.62
f_2	770	771.4	+0.19
f_3	852	857.2	+0.61
f_4	941	935.1	−0.63
f_5	1209	1215.9	+0.57
f_6	1336	1331.7	−0.32
f_7	1477	1471.9	−0.35
f_8	1633	1645.0	+0.73

Any crystal frequency deviation from 3.579545 MHz will be reflected in the tone output frequency. Most crystals don't vary more than ± 0.02%.

Op Amp Out (Pin 1)

The Op Amp Out pin is connected internally in the SBA5091 to the CMOS output transistor of an operational amplifier. This operational amplifier mixes an output level referenced to the supply voltage.

Bipolar Input (Pin 17)

The Bipolar Input pin is connected internally in the SBA5091 to the base of a un-committed on-chip bipolar transistor. This transistor is generally used to construct a multi-pole filter for low distortion applications.

Bipolar Output (Pin 18)

The Bipolar Output pin is connected internally in the SBA5091 to the emitter of the bipolar transistor described by the paragraph Bipolar Input, above.

Output Waveform

The row column output waveforms are shown in Fig. 5a and 5b. These waveforms are digitally synthesized using on-chip D-to-A converters. Distortion measurements of these unfiltered waveforms will show a typical distortion of 7% or less.

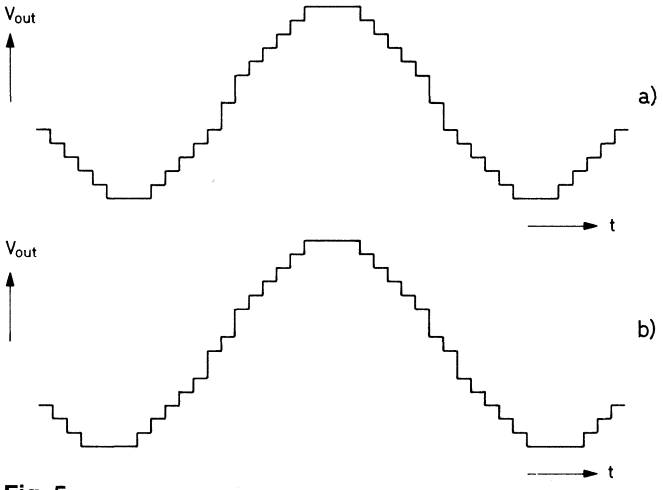


Fig. 5:
Typical sine wave output
a) Row tones
b) Column tones

The on-chip operational amplifier of the SBA5091 mixes the row and column tones together to result in a dual-tone waveform. Spectral analysis of this waveform will show that typically all harmonic and intermodulation distortion components will be −30 dB down when referenced to the strongest fundamental (column tone).

Fig. 6 an 7 show a typical dual-tone waveform and its spectral analysis.

Row and Column Inputs

The SBA5091 features inputs compatible with the standard 2-of-8 keyboard, the inexpensive single contact (form A) keyboard, and electronic input. Fig. 8a and 8b show how to connect to the two keyboard types, and Fig. 9 shows waveforms for electronic input. The inputs are static, i.e. there is no noise generation as occurs with scanned or dynamic inputs.

The internal structure of the SBA5091 inputs is shown in Fig. 10. R_{RI} and R_{CI} pull in opposite directions and hold their associated input sensing circuit turned off. When one or more row or column inputs are tied together, however, the Input Sensing Circuits sense the "1/2 Level" and deliver a logic signal to the internal circuitry of the SBA5091 and cause the

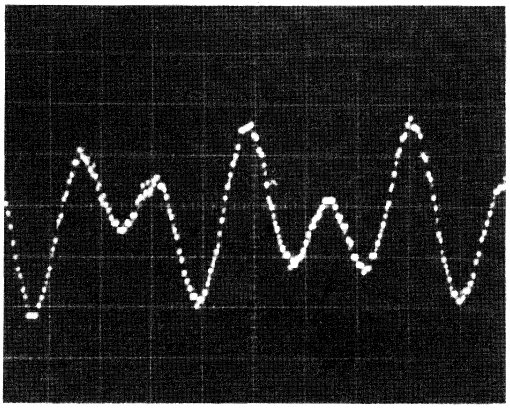


Fig. 6:
Typical dual-tone waveform (Row 1, Column 1)

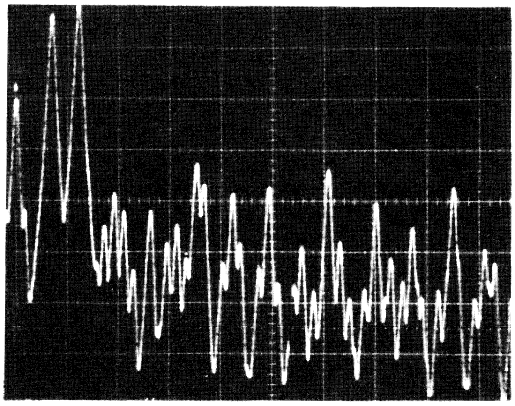


Fig. 7:
Spectral analysis of waveform in Fig. 6
(Vertical: 10 dB/Div., Horizontal: 1 kHz/Div.)

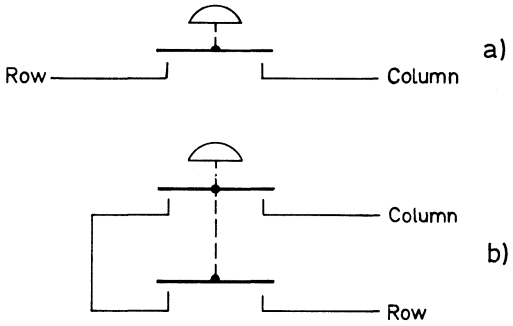


Fig. 8:
Keyboard configuration
a) Class A keyboard
b) 2-of-8 DTMF keyboard

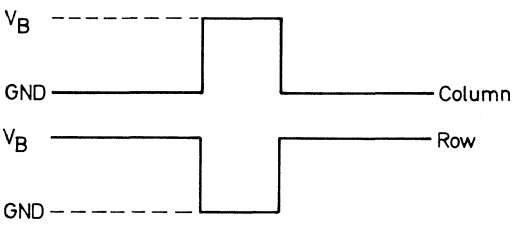


Fig. 9:
Electronic input pulses

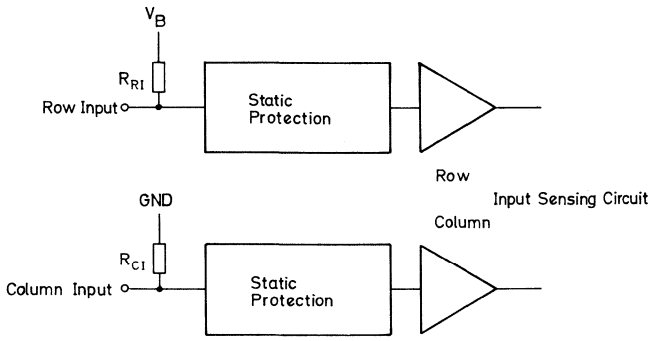


Fig. 10:
Internal structure of the row and column inputs

proper tone or tones to be generated. Typical input impedances of row and column pull-up resistors may be inferred from Fig.11.

When operating with a keyboard, normal operation would be for $\overline{\text{Single}}$ $\overline{\text{Tone}}$ $\overline{\text{Inhibit}}$ to be = "1". This allows single-tone operation when more than one button is activated. Activation of diagonal buttons will result in no tones being generated.

If a single tone is desired for test, but is not desired for operation, an external resistor can pull $\overline{\text{STI}}$ = Logic "0". This allows dual-tone operation with single key closure, but prevents any output tones when more than one button in the same row or column is activated.

When the inputs to the SBA5091 are electronically activated, per Fig. 9 input to a single row and column will result in that dual-tone digit's being generated. Input to a single column will result in that column-tone being generated. Input to multiple columns will result in no tone being generated.

Activation of a single row is not sensed by the internal circuitry of the SBA5091. If a single row tone is desired, two columns must be activated along with the desired row.

Fig. 11a:
Row or column input current versus input voltage
Full range

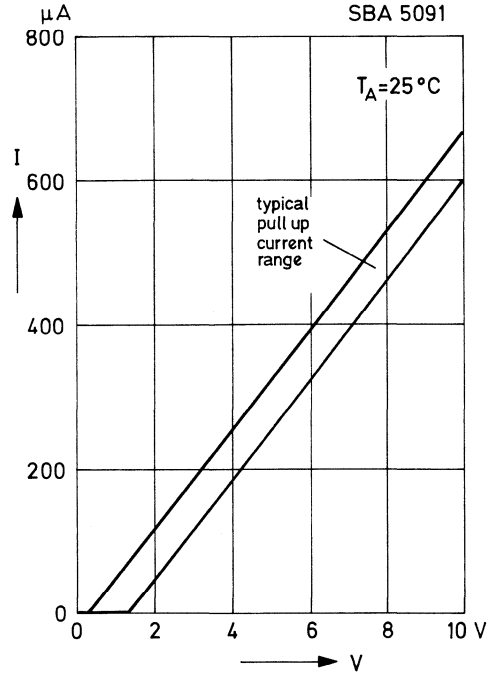
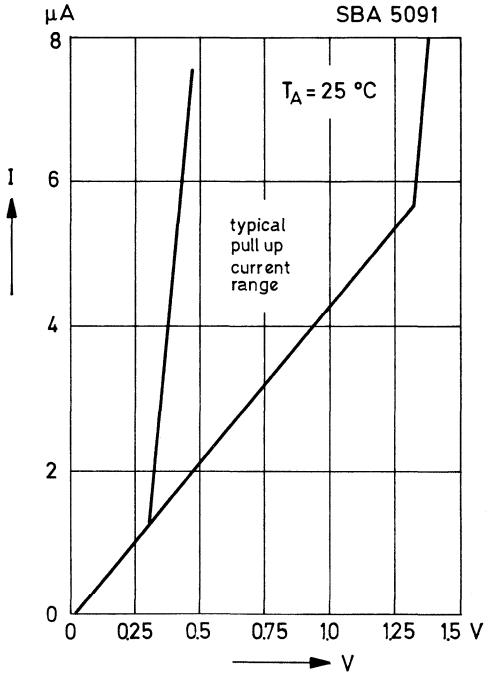


Fig. 11b:
Row or column input current versus input voltage
Extended range



Telephone Subset Amplifier

Features:

Automatic compensation of line losses by using a gain-controlled amplifier

Very accurate (±2 dB) send, receive and VF (voice frequency) gains to achieve optimum system performance

Low supply current obtained entirely from a small proportion of the line current

Contains cancellation circuit to achieve required reduction in sidetone

Balanced microphone input circuit for reduced sidetone

Operation can be achieved if the subsets are paralleled Stabilised D.C. output for powering external VF oscillator

Send, VF and receive gains can be preset externally by choice of resistors

Both low and high frequency characteristics (usually roll off's) of the send gain can be separately adjusted by external capacitors

Control of quiescent operating point on curve relating D.C. line current with amplifier gain

Low send and receive noise

Mute facility for send and receive amplifiers during dialling

General Description

The TEA 1045 is a bipolar integrated circuit specially designed for use in a telephone subset to amplify the output from the handset microphone to the telephone line and to amplify the incoming speech on the line to the earpiece transducer. The microphone and earpiece transducers can be of the same type and construction.

The diagram Fig. 1 shows the essential parts of the circuit. The output of the microphone is applied to the balanced input, pins 12 and 13. The signal is amplified and the output is obtained from pin 18 for further amplification by a transistor to the telephone line. The nominal gain of the amplifier is set by an external resistor on pin 6 with the low and high freqency characteristic controlled by external capacitors on pins 10 and 11 respectively. The gain of the amplifier is also controlled by the voltage on pin 7 connected to a resistive divider (R_{D1} and R_{D2}) across the telephone line.

The nominal voltage is set by a number of variables especially the resistive drop along the line. If the line resistance increases the voltage at pin 7 falls, increasing the gain of the amplifier to offset the A.C. transmission losses as these relate directly to the D.C. losses of the line. Received signals from the line are

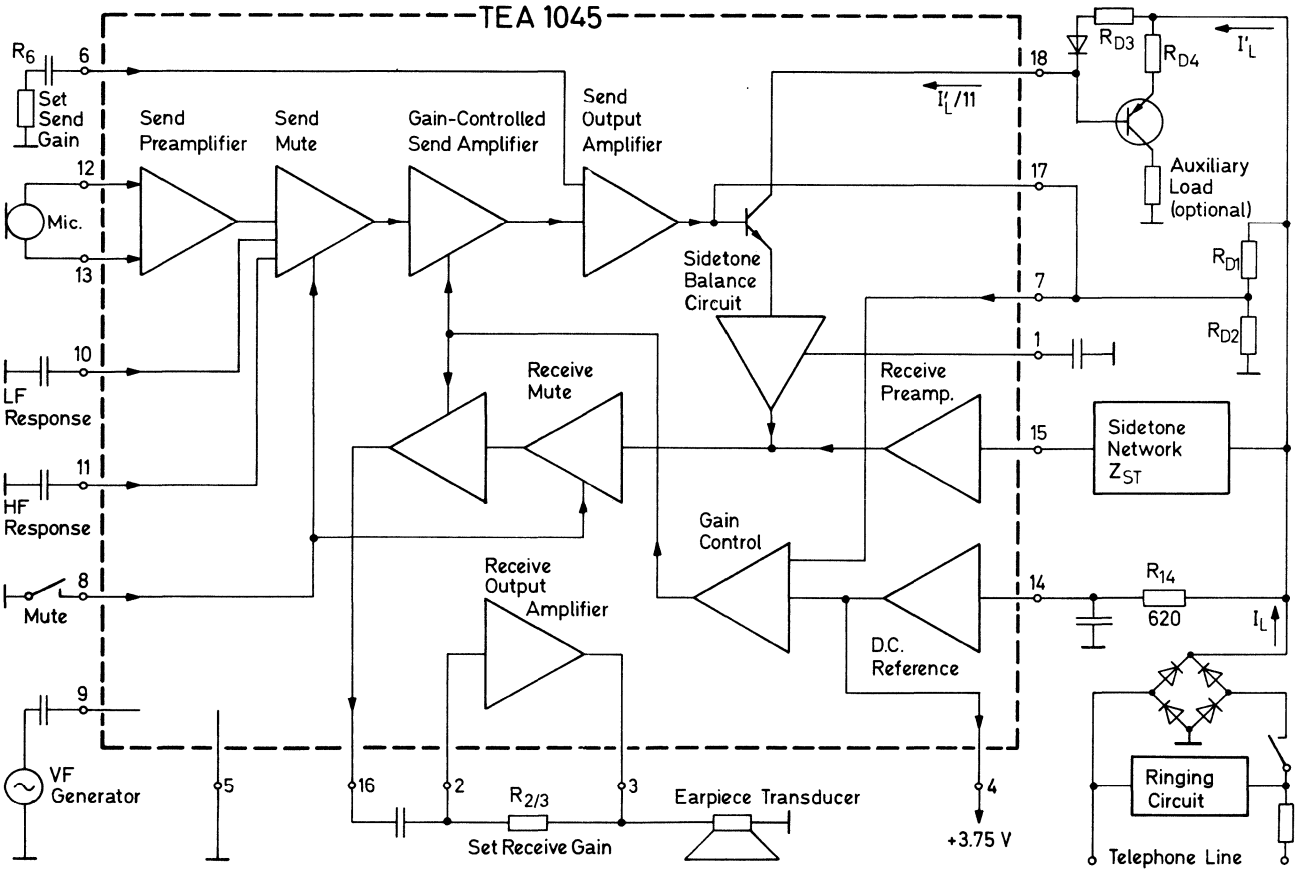
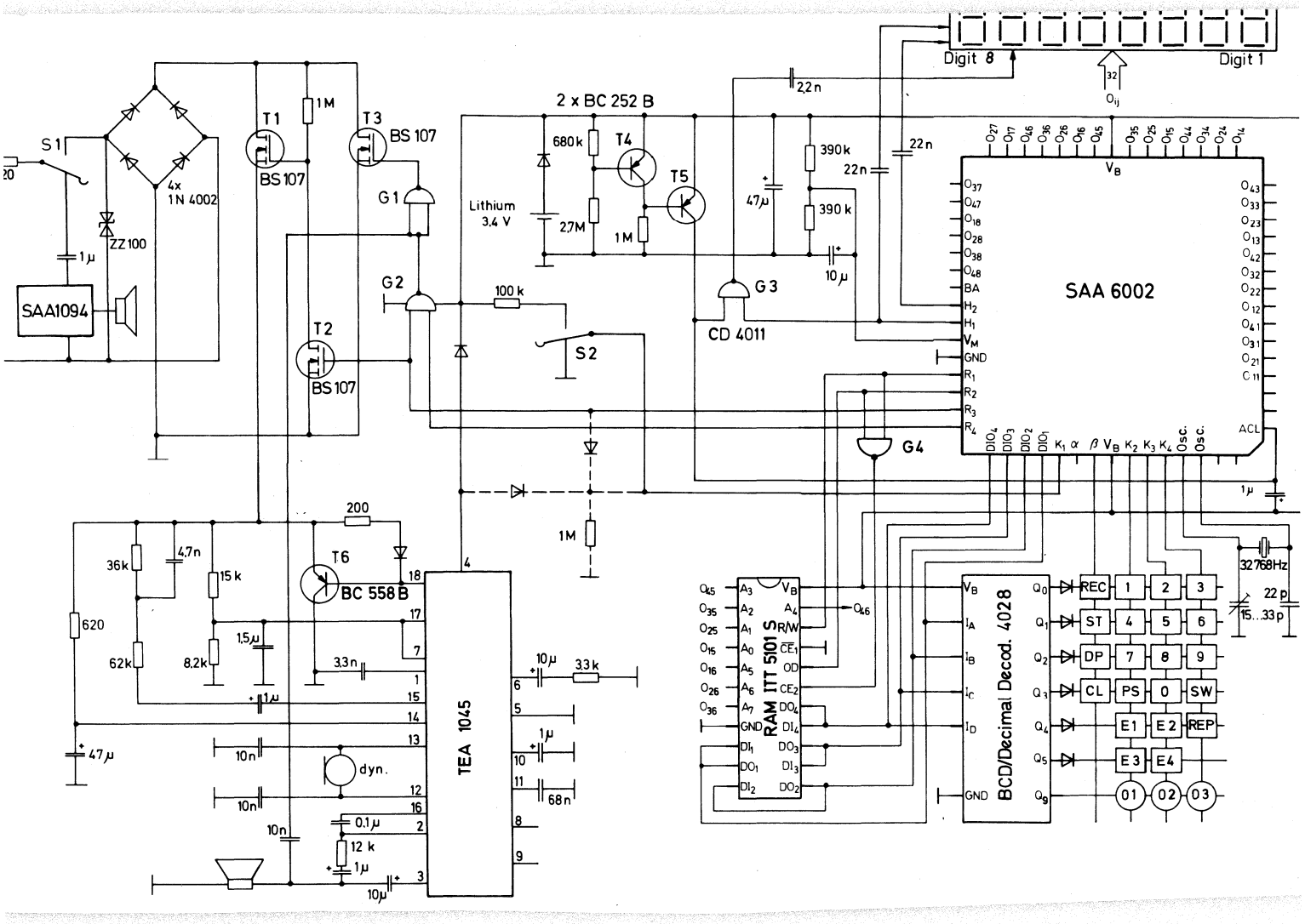


Fig. 1: TEA 1045 block diagram and application circuit


Digit 8
Digit 1
32
O_{ij}
2 x BC 252 B
2,2n
680k
T4
T5
390k
22n
22n
47µ
390 k
Lithium
3,4 V
2,7M
1M
10 µ
G3
CD 4011
SAA 6002
V_B
V_M
GND
BA
ACL
S1
4x
1N 4002
ZZ100
1 µ
SAA1094
T1
BS 107
1M
T3
BS 107
G1
G2
100 k
S2
T2
BS 107
G4
200
T6
BC 558 B
36k
4,7n
15 k
620
62k
8,2k
1,5µ
3,3n
1µ
47µ
10n
dyn.
10n
10n
0,1µ
12 k
1µ
10µ
TEA 1045
10µ
3,3k
1µ
68n
1M
RAM ITT 5101 S
BCD/Decimal Decod. 4028
REC
ST
DP
CL
PS
SW
REP
E1
E2
E3
E4
01
02
03
32768Hz
22 p
15...33 p

amplified after having been passed through a sidetone network connected to pin 15. The receive amplifier consists of two parts, a preamplifier whose gain is controlled by the length of the line as in the send amplifier, and a main output to feed the earpiece transducer. The gain of the output amplifier is set by a resistor between pins 2 and 3 acting as a feedback resistor.

The TEA 1045 is also designed to accomodate two-tone VF dialling signals. A separate VF generator IC can be powered by the stablised D.C. supply voltage available from pin 4 (nominally +3.8 V). The VF signal from the generator is applied to pin 9 and is amplified and mixed into part of the send amplifier. This amplifier is gain-controlled by the line current and the nominal gain is set by the resistance on pin 6. The gain of the VF amplifier is not affected by the capacitors on pins 10 and 11. Alternatively the VF signal can be fed into pin 6 if the gain control by the line is not desired.

When dialling, both the send and receive amplifiers can be muted by grounding the input to pin 8. An appropriate signal is usually obtained directly from the VF generator integrated circuit. The nominal muting exceeds 60 dB on send and 30 dB when receiving.

The overall characteristics of the TEA 1045 are very well defined and controlled. Both send and receive gains within the integrated circuit have only a small overall spread of 4 dB (±26% about nominal). With line impedance and set gain resistors closely controlled the performance of the subset is well defined in the system.

D.C. Interface to the line

A small portion of the D.C. line current is used to power the TEA 1045 via pin 14. However the external transistor in Fig. 1 divides the remainder of the line current such that one eleventh flows into pin 18 and serves as the D.C. current of the send output stage within the integrated circuit. This keeps the dissipation within the TEA 1045 low. The remainder of the line current flows through the collector of the external transistor to ground. If required there is sufficient voltage between the emitter of the transistor and ground to use this current to power an audio loudspeaker amplifier placed between the collector and ground. The D.C. voltage across the whole circuit directly relates to the D.C. line current and to the A.C. line losses. This nominal subset D.C. voltage is 12.6 V for a line current of 43 mA reducing on long telephone lines to 8.5 V with a line current of 17.5 mA. The tolerence on this voltage is about ±20% with reference to the nominal.

Gain setting

The nominal send gain is given by the following equation for a zero length line:

$$G_S = 195.6 \cdot \left(1 + \frac{R_{D3}}{R_{D4}}\right) \cdot \frac{R_L}{R_6}$$

Where R_L is the A.C. line impedance presented to the send signal. This is the line impedance (commonly 600 Ω) in parallel with R_{14} which can be 620 Ω to terminate the line. The resistor R_{D3} is chosen to be ten times the resistor R_{D4} for correct operation of the TEA 1045. If R_6 is 1 kΩ, the nominal voltage gain is 56.3 dB. For long lines this gain increases by about 5 dB.

The nominal receive gain includes the attenuation of the sidetone impedance network in series with pin 15 and is given by the following equation for a zero line:

$$G_R = 1.28 \frac{R_{2/3\,T}}{Z_{ST}}$$

where $R_{2/3\,T}$ is the total resistance between pin 2 and pin 3. This includes an external resistor used to preset the gain and an internal resistor of 450 kΩ within the TEA 1045. This equation approximates to:

$$G_R = 1.25 \frac{R_{2/3}}{Z_{ST}}$$

where $R_{2/3}$ is the total external resistance between pins 2 and 3. For long lines this gain increases by about 6 dB.

The gain from the VF input (pin 9) to the line has a nominal value given by the equation:

$$G_{VF} = 2.3 \cdot \left(1 + \frac{R_{D3}}{R_{D4}}\right) \cdot \frac{R_L}{R_6}$$

This gain varies with the line current in the same ratio as the send gain.

Sidetone

With the TEA 1045 a hybrid transformer is not required for sidetone cancellation since part of the transmitted speech signal is amplified and applied into the receive amplifier such as to cancel the unwanted coupling on the line between send and receive signals. A resistor-capacitor network in series with the receive input pin 15 is chosen to obtain nulling. The gain set resistors $R_{2/3}$ and R_6 do not affect the balance as they adjust the gain equally in both the send-receive loop and the internal nulling-signal path. With a nominal line impedance of 600 Ω the optimum impedance of the network is in the region of 50 kΩ to 100 kΩ. The capacitor-resistor network used depends very much on the rather subjective audio listening tests conducted on the subset in the specified transmission circuit.

The dynamic range of both the send and receive gain-control circuits is restricted to reduce the effect of objectionable sidetone on very long lines. A capacitor applied between pin 1 and ground can correct for the relative phase error between the send-receive loop and the sidetone nulling-signal for better sidetone balance.

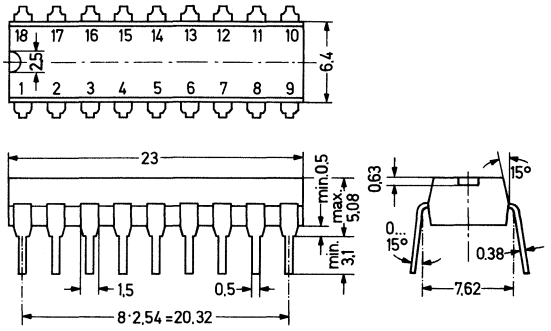


Fig. 2:
TEA 1045 in an 18-pin Dil plastic package, 20A18 according to DIN 41866

Weight approx. 1.5 g
Dimensions in mm

Pin Connections

1	Side tone balance capacitor pin
2	Receive gain setting input
3	Receive output
4	Reference voltage output
5	Ground
6	Send gain setting input
7	Loop equalization input
8	Mute input
9	Voice frequency (VF) input
10	Roll-off Low input
11	Roll-off High input
12	Send input
13	Send input
14	Supply voltage
15	Receive input
16	Receive pre-amp output
17	D.C. slope pin
18	Send output

All voltages are referred to Pin 5.

Absolute Maximum Ratings

	Symbol	Value	Unit	
Supply Voltage Pin 18	V_{18}	20	V	
Pin 4	V_4	15	V	
Line Current	I_L	9 to 80	mA	
Power Dissipation	P_{tot}	290	mW	
Ambient Operating Temperature Range	T_A	−25 to +55	°C	
Storage Temperature Range	T_S	−40 to +70	°C	

D.C. Characteristics and Operating Conditions at $V_{14} = 8$ V, $I_{18} = 1.75$ mA

	Symbol	Min.	Max.	Unit	Conditions
Supply Current	I_{14}	2.2	5.2	mA	–
Supply Voltage	V_4	3.75	4.05	V	$I_4 = 0.1$ mA
	V_4	3.65	3.95	V	$I_4 = 1.5$ mA
Send Quiescent Voltage	V_1	1.05	1.65	V	$I_4 = 1.5$ mA
Receive Quiescent Voltage	V_{16}	2.65	3.85	V	
Receive Quiescent Output Voltage	V_3	0.95	1.65	V	
Imput Mute Current	$-I_8$	–	0.23	mA	

A.C. Tests at $V_{14} = 8$ V, $I_{18} = 4.35$ mA, f = 7 kHz, in the test circuit Fig. 3 unless otherwise stated

	Symbol	Min.	Typ.	Max.	Unit	Conditions
Send Gain	G_S	54.1	–	58.1	dB	$R_L = 3.23\ k\Omega$, $V_{12/13} = 0.57$ mV RMS
Receive Gain	G_R	−17.0	–	−13.0	dB	$I_{15} = 27.7\ \mu A$ RMS
VF Gain to Output	G_{VF}	15.6	–	19.6	dB	$V_9 = 47$ mV RMS
Send Noise	N_S	–	500	–	μV	$I_{18} = 1.75$ mA, Test Circuit Fig. 4
Receive Noise	N_R	–	300	–	μV	$I_{18} = 1.75$ mA

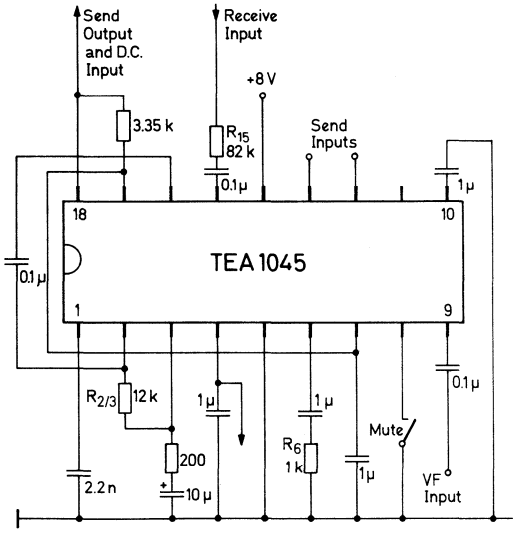


Fig. 3: A.C. test circuit

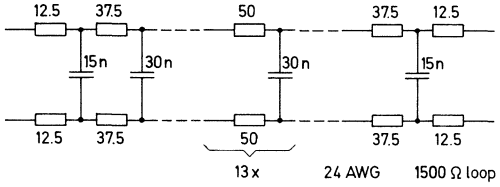


Fig. 5: Artifical cable circuit

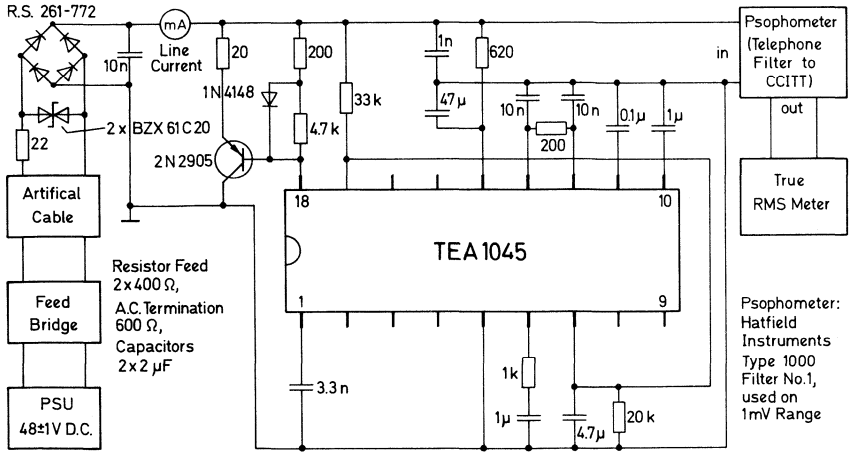


Fig. 4: Noise test circuit

Speech Generator

MOS one-chip speech generator IC in N-channel Silicon-gate technology, mask-programmable for different languages and vocabularies. Application fields for such low-cost speech generators are speech output in clocks, telephone answering equipment, status and emergency signalling etc.

The storage and processing of the speech elements is completely digitized. By combining several complex methods of data reduction and removing recundancy it became possible to accomodate the required memory capacity for a vocabulary of about 20 words as well as control, decoding and D/A converting functions on one single MOS chip.

Each word generated by the speech generator consists of a number of staircase-shaped pulses having a fixed period of 10 ms. Each pulse is built up from 128 steps. The smallest amplitude variation is one sixteenth of the peak amplitude. This means 4 bit amplitude information. Depending on digital control signals, the stored vocabulary is combined into different phrases.

The first mass-produced version of the speech generator is the type UAA1003-1. This device is programmed for announcement of time in a talking clock, in the German language. This IC converts the time information (delivered by a digital electronic clock in seven-segment code) into a spoken time announcement. In addition, an alarm signal is generated on-chip.

At the alarm time which has been set at the clock IC, first the alarm tone sounds and thereafter the clock speaks the sentence: "Es ist . . . Uhr . . .". In the simplest case, the amplitude of the alarm tone is constant. By means of a small additional network a gong sound of decreasing amplitude can be achieved.

The version UAA1003-2 is programmed for French language time announcements, whereas the type UAA1003-3 will speak English.

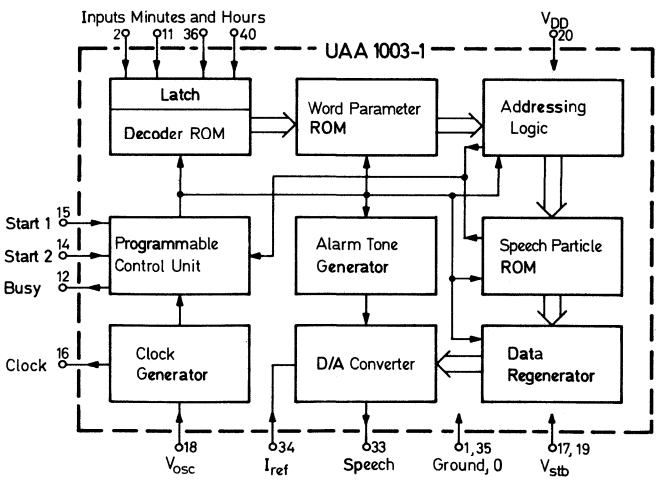


Fig. 1:
Block diagram of the speech generator UAA1003-1

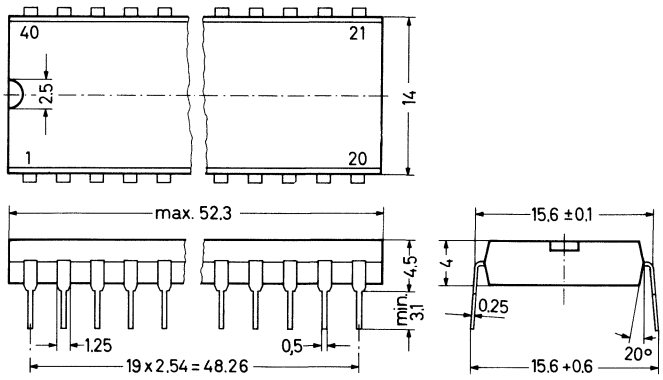


Fig. 2:
UAA1003 in 40-pin
Dil plastic package, 20 B 40
according to DIN 41866

Weight approximately 6 g
Dimensions in mm

Pin Connections of the UAA1003-1

1	Ground, 0, V_{SS}
2	Input hours units b
3	Input hours units a
4	Input minutes tens f
5	Input minutes tens e
6	Input minutes tens d
7	Input minutes units g
8	Input minutes units f
9	Input minutes units e
10	Input minutes units b
11	Input minutes units a
12	Busy output
13	Test pin, leave vacant
14	Start 2 input
15	Start 1 input
16	Clock frequency output
17	Standby supply voltage V_{stb}
18	Oscillator frequency adjust input
19	Standby supply voltage V_{stb}
20	Supply voltage V_{DD}
21 to 32	Test pins, leave vacant
33	Speech output
34	Reference current input
35	Ground, 0, V_{SS}
36	Input hours tens g
37	Input hours tens f
38	Input hours units g
39	Input hours units f
40	Input hours units e

All voltages are referred to pin 1.

Absolute Maximum Ratings

	Symbol	Value	Unit
Supply Voltages	V_{DD}	10	V
	V_{stb}	10	V
Voltage at the other Pins	V_n	−0.3 to 10	V
Drain Currents, Pins 12 and 16	I_D	5	mA
Output Current, Pin 33	I_{out}	5	mA
Ambient Operating Temperature Range	T_A	−20 to +65	°C
Storage Temperature Range	T_S	−55 to +125	°C

Recommended Operating Conditions

	Symbol	Min.	Typ.	Max.	Unit
Supply Voltages					
Pin 20	V_{DD}	4.5	5	5.5	V
Pins 17 + 19, Circuitry as shown in Fig. 4	V_{stb}		V_{DD} +1 V		–
Pins 17 + 19, without Standby Operation, connected to Pin 20	V_{stb}	–	= V_{DD}	–	–
Oscillator Frequency Adjustment Voltage	V_{osc}	0	–	V_{DD}	–
Input Voltage, Pins 2 to 11, 14, 15, and 36 to 40	V_{IH}	1.5 V	–	V_{DD}	–
	V_{IL}	–	–	0.3	V
Reference Current, Pin 34	I_{ref}	–	50	–	μA
obtainable Voltage at Pin 34 (see Page 3)	V_{34}	2.5	–	–	V
Output Load Resistance, Pin 33	R_L	–	–	680	Ω

Characteristics at V_{DD} = 5 V, I_{ref} = 50 μA, T_A = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Current Consumption					
Standby Supply	$I_{17} + I_{19}$	–	2	–	mA
Pin 20 when speaking	I_{20}	–	25	–	mA
Max. Output Current when speaking	I_{33}	–	750	–	μA
Voltage Drop Across the Open-Drain Output Transistors					
Pin 12 at I_D = 1 mA	$\triangle V_{12}$	–	–	0.3	V
Pin 16 at I_D = 1 mA	$\triangle V_{16}$	–	–	0.7	V
internal Oscillator Frequency	f_{osc}	–	230.4	–	kHz
Clock Frequency at Pin 16	f_t	–	25.6	–	kHz
Alarm Tone Frequency (from Pin 33)	f_{al}	–	800	–	Hz

Operation Mode of the UAA1003-1

When the speech generator is activated via one of the two start inputs, the input information is stored. The chosen phrase is defined by the decoder ROM and the programmable control unit. These together address the corresponding word parameters which cause the addressing logic to read the speech particles from the speech particle ROM. The digital-coded sequence of the speech particles is processed in the data regenerator and fed to the D/A converter, which delivers the speech signal at its output.

Connections of the UAA 1003-1 and their Function

Pins 2 to 11 and 36 to 40 – Data inputs
The data inputs of the UAA1003-1 are directly connected to the anodes of the seven segment display, assuming that the cathodes are connected to V_{SS}; see Fig. 4. Table 1 shows the relationship between the segments and the number to be spoken, and in Fig. 3 the letters belonging to the seven segments are shown. Not all seven segments are needed for decoding the time indicated by the clock (see table 1).

Table 1: Coordination between numbers and segments

Minutes and Hours Units

Decimal Number	Segments a	b	e	f	g
0	1	1	1	1	0
1	0	1	0	0	0
2	1	1	1	0	1
3	1	1	0	0	1
4	0	1	0	1	1
5	1	0	0	1	1
6	1	0	1	1	1
7	1	1	0	0	0
8	1	1	1	1	1
9	1	1	0	1	1

Minutes Tens

Decimal Number	Segments d	e	f
0	1	1	1
1	0	0	0
2	1	1	0
3	1	0	0
4	0	0	1
5	1	0	1

Hours Tens

Decimal Number	Segments f	g
0	1	0
1	0	0
2	0	1

1 = LED activated, 0 = LED off

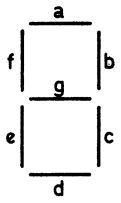


Fig. 3:
Designation of the segments at seven segment displays

Pin 12 – Busy output
Connected to this output is the drain terminal of an open-drain transistor. This is conducting during the entire speech time. By means of the Busy signal external circuitry can be controlled. As an example, the supply voltage V_{DD} can be turned on via the Busy signal (see Fig. 4).

Pin 14 – Start 2 input
If a positive pulse of at least 10 μs is applied to pin 14, the control unit is started for the phrase "Es ist . . . Uhr . . .", without preceding alarm tone being produced, and the Busy output becomes Low-impedance. There is, however, an interval of 1 s between start pulse and beginning of speech output.

Pin 15 – Start 1 input
If a positive pulse of at least 10 μs is applied to pin 15, first an alarm tone will sound for about 1 s, and thereafter the phrase "Es ist . . . Uhr . . ." will be spoken. The Busy output becomes Low-impedance when the alarm tone begins.

Pin 16 – Clock frequency output
At this pin, the internal clock frequency which determines the pitch of the voice can be measured. The output transistor is an open-drain transistor.

Pins 17 and 19 – Standby supply voltage
These pins serve for supplying the oscillator, the initializing circuit (not shown in the block diagram) and the start input circuit. These parts of the UAA1003-1 are powered continuously, whilst the residual part of the IC which is powered via pin 20 can be switched off when not speaking. Thus a smaller consumption can be achieved in the standby mode.

Pin 18 – Oscillator frequency adjust input
To this pin a variable voltage of 0 to +5 V must be applied in order to adjust the clock frequency which can be measured at pin 16 to the value of 25.6 kHz.

Pin 20 – Supply voltage V_{DD}
As mentioned with pins 17 and 19, the major part of the UAA1003-1 is powered via pin 20, except for the standby-powered part. Thus a small consumption can be achieved in the standby mode. As can be seen in Fig. 4, the transistor switch for the supply of pin 20 is controlled by the Busy output pin 12.

Pin 33 – Speech output
This output delivers the speech signal in the shape of an output current. By means of a load resistor of 680 Ω to V_{DD} this current is converted into an output voltage having an amplitude of 0.5 V p–p maximum. After suppressing the clock signal in a simple external bandpass filter the analog speech signal is obtained. The filter should be composed of a highpass network (f_u = 300 Hz) and two lowpass networks (f_{O1} = 1.5 kHz and f_{O2} = 3.5 kHz). By varying the filter cutoff frequencies the subjective sound impression can be optimized.

Pin 34 – Reference current input
To this input must be applied an externally produced reference current. The variation of this current causes a linear variation of the output current delivered by pin 33 and hence a variation of the speech or alarm signal amplitude. Care must be taken that the current source which produces the reference current is able to deliver an output voltage of a least 2.5 V under worst case conditions.

If a current source according to Fig. 4 is provided, and the speech IC becomes activated by means of a start pulse applied to pin 14 or pin 15, the reference current input pin 34 gets a current pulse which decreases exponentially to the nominal value of the reference current. If the start pulse is applied to pin 15 (Start 1) there will be produced an alarm tone which decreases like a gong, and thereafter the time will be spoken. If the start pulse is applied to pin 14 (Start 2) the reference current decreases in the 1 s pause which occurs in front of the spoken time announcement. The capacitance of the timing capacitor must be chosen so that at the end of the alarm tone, 1 s after the start pulse, the reference current reaches its nominal value.

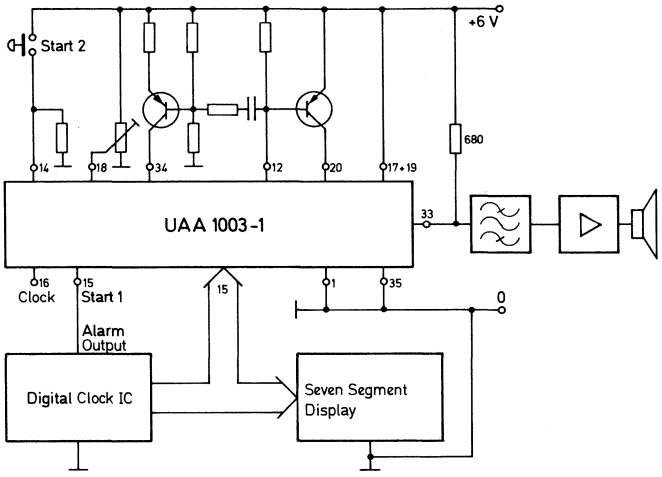
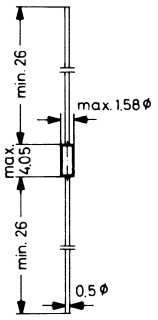


Fig. 4:
Application circuit of the UAA1003-1 in a talking alarm clock

ZSY0,7

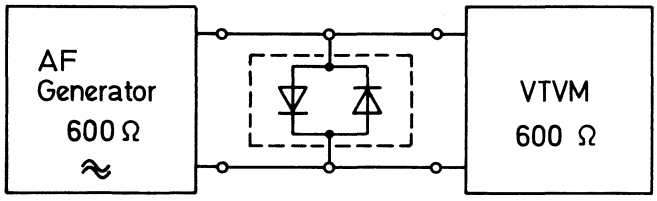
Silicon Click Suppressor

Monolithic integrated analog circuit with symmetric V/I-characteristic for use in voltage limiter circuits, e.g. as click suppressor in telephone sub-sets.



Glass case JEDEC DO-35
54 A 2 according to DIN 41880

Weight approximately 0.13 g
Dimensions in mm



Test Circuit

Absolute Maximum Ratings

	Symbol	Value	Unit	Conditions
Operating Current	$\pm I_F$	150	mA	$T_A = 25$ °C
Surge Current	$\pm I_{FSM}$	1	A	t = 100 μs
Power Dissipation	P_{tot}	300	mW	$T_A = 25$ °C
Junction Temperature	T_j	150	°C	
Storage Temperature Range	T_S	–55 to +150	°C	

Characteristics at $T_A = 25$ °C

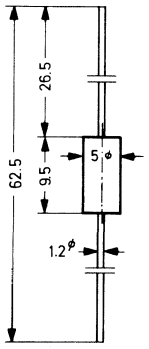
	Symbol	Min.	Typ.	Max.	Unit	Conditions
Voltage Drop	$\|V_F\|$	550	–	680	mV	$\|I_F\| = 50\ \mu$A
	$\|V_F\|$	650	–	810	mV	$\|I_F\| = 2$ mA
	$\|V_F\|$	–	–	1.35	V	$\|I_F\| = 100$ mA
Dynamic Resistance	r_f	11	20	29	Ω	$\|I_F\| = 2$ mA, f = 1 kHz
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	400	°C/W	
Residual Attenuation D in the test circuit shown above at a real 600 Ω ± 5% generator output resistance as well as VTVM input resistance, VTVM having full wave rectification with quadratic characteristic						Voltage Level at the Generator (with click suppressor under test)
	D	–	0	0.05	N	– 4 N
	D	–	0	0.05	N	– 2 N
	D	–	0.05	–	N	– 0.5 N
	D	–	0.5	–	N	– 0.2 N
	D	0.5	1.8	–	N	0 N

ZZ16 . . . ZZ160

Bidirectional Zener Diodes

Features:

- High energy absorption in both directions
- Extremely fast response
- Especially designed to protect telephone circuits and other voltage-sensitive devices including semiconductors



Plastic case ≈ DO-13

Weight approximately 1 g
Dimensions in mm

All parameters are valid for both current directions.

Characteristics at T_j = 25 °C

Type	Zener voltage at I_Z = 5 mA V_Z V*		Temperature coefficient of Zener voltage at I_Z = 5 mA α_{VZ} 10^{-4}/°C		Reverse voltage at I_R = 5 μA V_R V**	Capacitance at V_R = 0, f = 1 MHz C_{tot} pF
	min.	max.	min.	max.	min.	typ.
ZZ 16	13	20	4	10	10	1800
ZZ 36	29.6	43.5	5	11	25	700
ZZ 62	50	75	6	12	42	450
ZZ 160	130	200	6	12	110	200

Type	Voltage drop at pulses 8/20 V_p V	Voltage drop at pulses 10/1000 V_p V
	max.	max.
ZZ 16	30	25
ZZ 36	60	53
ZZ 62	105	90
ZZ 160	255	235

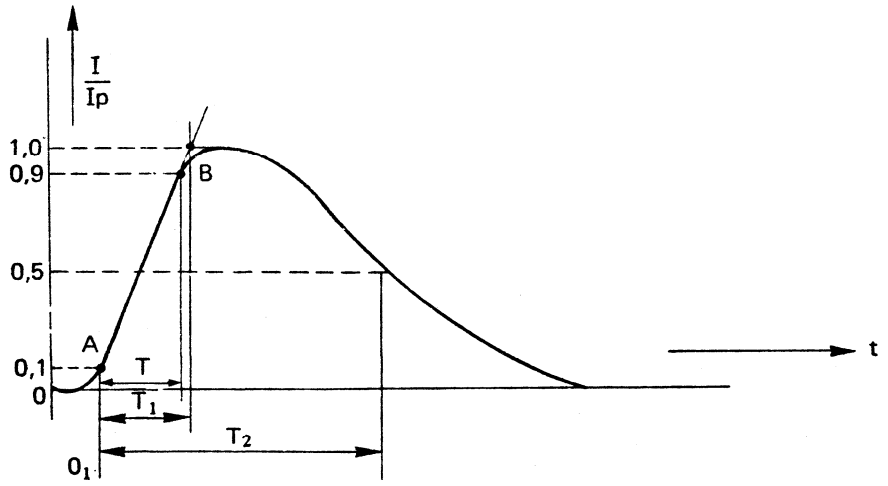
* tested with pulses
** maximum recommended supply voltage of the equipment to be protected

Maximum Ratings

Junction temperature	T_j	max. 150 °C
Storage temperature range	T_S	–55 to +155 °C

Power rating by current pulses, starting from T_j = 25 °C, at a pulse rate frequency of ≤ 0.1 Hz and a pulse shape according to the curve shown below, tested with pulses 8/20 (T_1 = 8 μs T_2 = 20 μs) and with pulses 10/1000 (T_1 = 10 μs, T_2 = 1000 μs). The maximum voltage drop across the diode at these pulse currents is listed on page 2. Any diode destroyed by overload shows a short-circuit caused by through-alloying the junction.

Type	permissible pulse current at pulses 8/20 I_p A	permissible pulse current at pulses 10/1000 I_p A
ZZ 16	max. 300	max. 30
ZZ 36	max. 130	max. 13
ZZ 62	max. 80	max. 8
ZZ 160	max. 30	max. 3

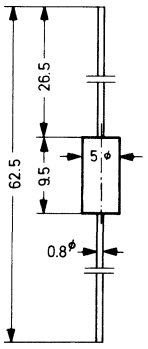


ZZY16 . . . ZZY160

Bidirectional Zener Diodes

Features:

- High energy absorption in both directions
- Extremely fast response
- Especially designed to protect telephone circuits and other voltage-sensitive devices including semiconductors



Plastic case ≈ DO-13

Weight approximately 0.8 g
Dimensions in mm

All parameters are valid for both current directions.

Characteristics at $T_j = 25°C$

Type	Zener voltage at $I_Z = 5$ mA V_Z V*		Temperature coefficient of Zener voltage at $I_Z = 5$ mA α_{VZ} $10^{-4}/°C$		Reverse voltage at $I_R = 5\ \mu A$ V_R V**	Capacitance at $V_R = 0$, f = 1 MHz C_{tot} pF
	min.	max.	min.	max.	min.	typ.
ZZY 16	13	20	4	10	10	1200
ZZY 36	29.6	43.5	5	11	25	500
ZZY 62	50	75	6	12	42	300
ZZY 160	130	200	6	12	110	150

Type	Voltage drop at pulses 8/20 V_p V	Voltage drop at pulses 10/1000 V_p V
	max.	max.
ZZY 16	35	30
ZZY 36	75	65
ZZY 62	125	110
ZZY 160	305	285

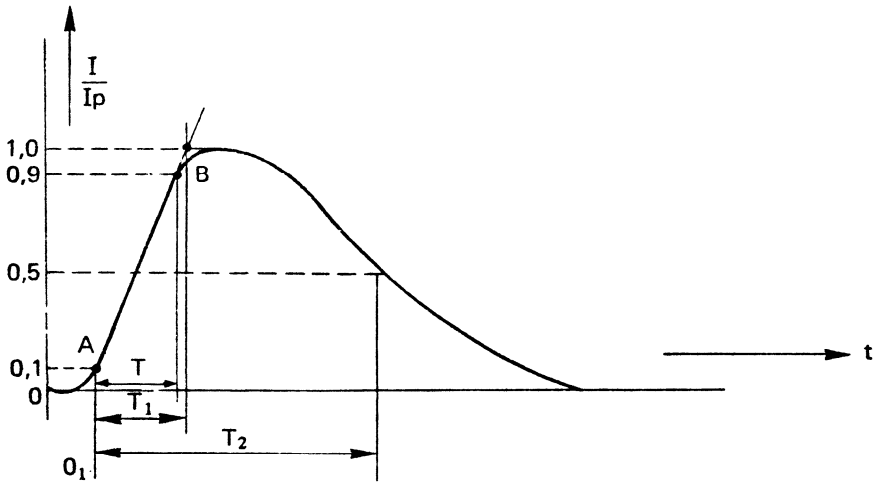
* tested with pulses
** maximum recommended supply voltage of the equipment to be protected

Maximum Ratings

Junction temperature	T_j	max. 150 °C
Storage temperature range	T_S	–55 to +155 °C

Power rating by current pulses, starting from T_j = 25 °C, at a pulse rate frequency of ≤ 0.1 Hz and a pulse shape according to the curve shown below, tested with pulses 8/20 (T_1 = 8 μs, T_2 = 20 μs) and with pulses 10/1000 (T_1 = 10 μs, T_2 = 1000 μs). The maximum voltage drop across the diode at these pulse currents is listed on page 2. Any diode destroyed by overload shows a short-circuit caused by through-alloying the junction.

Type	permissible pulse current at pulses 8/20 I_p A	permissible pulse current at pulses 10/1000 I_p A
ZZY 16	max. 200	max. 20
ZZY 36	max. 90	max. 9
ZZY 62	max. 60	max. 6
ZZY 160	max. 20	max. 2



BS170, BS250

Enhancement Mode VMOS Transistors

BS 170: N-Channel Type
BS 250: P-Channel Type

Features:

High input impedance
High speed switching
No minority carrier storage time
CMOS logic compatible input
No thermal runaway
No secondary breakdown

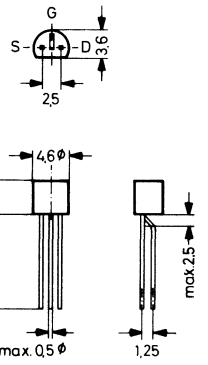


Fig 1:
Plastic Package TO-92

Weight approx. 0.18 g
Dimensions in mm

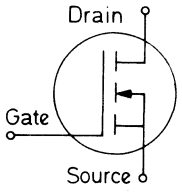


Fig. 2:
Diagram BS 170

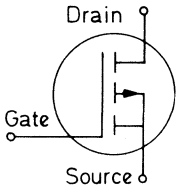


Fig. 3:
Diagram BS 250

Absolute Maximum Ratings

	Symbol	Value		Unit
		BS 170	**BS 250**	
Maximum Drain-Source Voltage	V_{DSS}	60	–45	V
Maximum Drain-Gate Voltage	V_{DGS}	60	–45	V
Maximum Continuous Drain Current	I_D	0.5	–0.5	A
Max. Power Dissipation at T_C = 25 °C	P_{tot}	0.83		W
Temperature (Operating and Storage)	T_j, T_S	–55 to +150		°C

Static Characteristics BS 170 at T_j = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at I_D = 100 μA, V_{GS} = 0	BV_{DSS}	60	90	–	V
Gate Threshold Voltage at V_{GS} = V_{DS}, I_D = 1 mA	$V_{GS(th)}$	0.8	–	3.0	V
Gate-Body Leakage Current at V_{GS} = 15 V, V_{DS} = 0	I_{GSS}	–	–	10	nA
Drain Cutoff Current at V_{DS} = 25 V, V_{GS} = 0	$I_{D(off)}$	–	–	0.5	μA
Drain-Source ON Resistance* at V_{GS} = 10 V, I_D = 0.2 A	$r_{DS(on)}$	–	3.5	5.0	Ω
Thermal Resistance Chip to Ambient Air	R_{thA}	–	150	–	°C/W

* Pulse Test Width – 80 μs; Pulse Duty Factor 1%.

Dynamic Characteristics BS 170 at T_j = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Forward Transconductance* at V_{DS} = 10 V, I_D = 0.2 A, f = 1 MHz	g_m	–	200	–	mS
Input Capacitance at V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	C_{iss}	–	60	–	pF
Turn ON Time at I_D = 0.2 A	t_{ON}	–	4	10	ns
Turn OFF Time at I_D = 0.2 A	t_{OFF}	–	4	10	ns

Static Characteristics BS 250 at T_j = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $-I_D$= 100 μA, V_{GS} = 0	$-BV_{DSS}$	45	70	–	V
Gate Threshold Voltage at V_{GS} = V_{DS}, $-I_D$ = 1 mA	$-V_{GS(th)}$	1.0	–	3.5	V
Gate-Body Leakage Current at $-V_{GS}$ = 15 V, V_{DS} = 0	$-I_{GSS}$	–	–	20	nA
Drain Cutoff Current at $-V_{DS}$ = 25 V, V_{GS} = 0	$-I_{D(off)}$	–	–	0.5	μA
Drain-Source ON Resistance* at $-V_{GS}$ = 10 V, $-I_D$ = 0.2 A	$r_{DS(on)}$	–	9	14	Ω
Thermal Resistance Chip to Ambient Air	R_{thA}	–	150	–	°C/W

Dynamic Characteristics BS 250 at T_j = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Forward Transconductance* at $-V_{DS}$ = 10 V, $-I_D$ = 0.2 A, f = 1 MHz	g_m	–	150	–	mS
Input Capacitance at $-V_{DS}$ = 10 V, V_{GS} = 0, f = 1 MHz	C_{iss}	–	60	–	pF
Turn ON Time at $-I_D$ = 0.2 A	t_{ON}	–	4	10	ns
Turn OFF Time at $-I_D$ = 0.2 A	t_{OFF}	–	4	10	ns

* Pulse Test Width – 80 μs; Pulse Duty Factor 1%.

BD512, BD522

Enhancement Mode Power VMOS Transistors
for applications needing high input impedance and fast switching times.

BD 512: P-channel transistor
BD 522: N-channel transistor

Features:

High input impedance
High speed switching
No minority carrier storage time
CMOS logic compatible input
No thermal runaway
No secondary breakdown
Paralleling is simple
Heat sink connected to drain

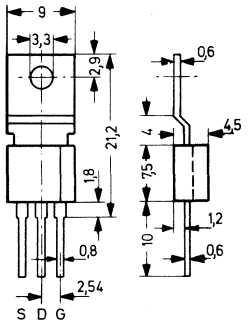


Fig. 1:
Plastic case TO-202
(34 A 3, DIN 41 869)

Weight approx. 1.5 g
Dimensions in mm

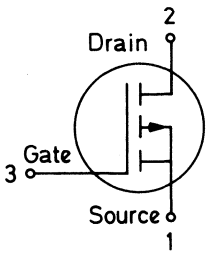


Fig. 2:
Diagram BD512

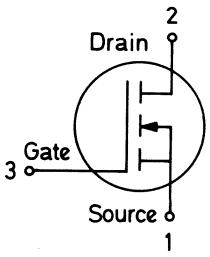


Fig. 3:
Diagram BD522

Absolute Maximum Ratings

	Symbol	Value		Unit
		BD 512	**BD 522**	
Drain-Source Voltage	V_{DSS}	–60	60	V
Drain-Gate Voltage	V_{DGS}	–60	60	V
Continuous Drain Current	I_D	–1.5	1.5	A
Power Dissipation				
at 25 °C Case Temperature	P_{tot}	10		W
at 25 °C Free Air Temperature	P_{tot}	1.75		W
Temperature (Operating + Storage)	T_j, T_S	–55 to +150		°C

Static Characteristics BD 512 at $T_j = 25\ °C$

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $V_{GS} = 0, -I_D = 100\ \mu A$	$-BV_{DSS}$	60	80	–	V
Gate Threshold Voltage at $V_{GS} = V_{DS}, -I_D = 1\ mA$	$-V_{GS(th)}$	1.0	–	3.5	V
Gate-Body Leakage Current at $-V_{GS} = 15\ V, V_{DS} = 0$	$-I_{GSS}$	–	–	100	nA
Drain Cutoff Current at $V_{GS} = 0, -V_{DS} = 25\ V$	$-I_{D(off)}$	–	–	0.5	μA
Drain-Source ON Resistance* at $-V_{GS} = 10\ V, -I_D = 1\ A$	$r_{DS(on)}$	–	4.5	7	Ω
Thermal Resistance					
Chip to Heat Sink	R_{thS}	–	–	12.5	°C/W
Chip to Ambient Air	R_{thA}	–	–	70	°C/W

Dynamic Characteristics BD 512 at $T_j = 25\ °C$

	Symbol	Min.	Typ.	Max.	Unit
Forward Transconductance* at $-V_{DS} = 10\ V, -I_D = 0.5\ A, f = 1\ MHz$	g_m	–	300	–	mS
Input Capacitance at $V_{GS} = 0, -V_{DS} = 10\ V, f = 1\ MHz$	C_{iss}	–	140	–	pF
Turn ON Time	t_{ON}	–	4	10	ns
Turn OFF Time	t_{OFF}	–	4	10	ns

* Pulse Test Width – 80 μs, Pulse Duty Factor 1%.

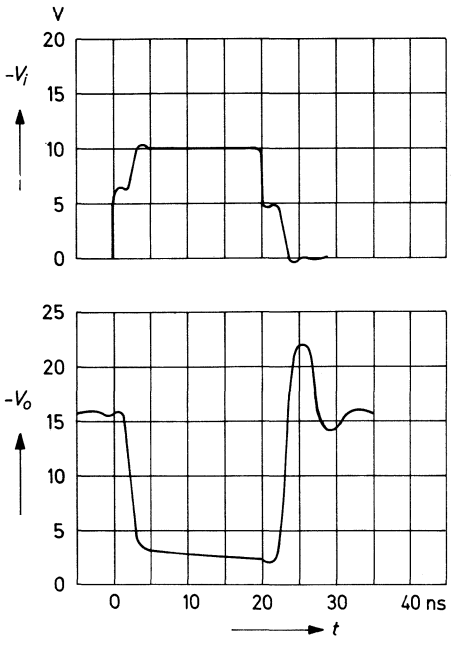


Fig. 4: Switching Performance of Input and Output Voltages (BD 512)

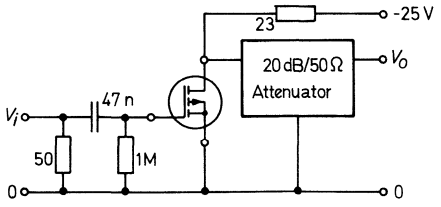


Fig. 5: Test Circuit for the Switching Times (BD 512)

Static Characteristics BD 522 at T_j = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at V_{GS} = 0, I_D = 100 μA	BV_{DSS}	60	90	–	V
Gate Threshold Voltage at V_{GS} = V_{DS}, I_D = 1 mA	$V_{GS(th)}$	0.8	–	3.0	V
Gate-Body Leakage Current at V_{GS} = 15 V, V_{DS} = 0	I_{GSS}	–	–	100	nA
Drain Cutoff Current at V_{GS} = 0, V_{DS} = 25 V	$I_{D(off)}$	–	–	0.5	μA
Drain-Source ON Resistance* at V_{GS} = 10 V, I_D = 1 A	$r_{DS(on)}$	–	2.0	3.0	Ω
Thermal Resistance					
Chip to Heat Sink	R_{thS}	–	–	12.5	°C/W
Chip to Ambient Air	R_{thA}	–	–	70	°C/W

Dynamic Characteristics BD 522 at T_j = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Forwards Transconductance* at V_{DS} = 10 V, I_D = 0.5 A, f = 1 MHz	g_m	–	400	–	mS
Input Capacitance at V_{GS} = 0, V_{DS} = 10 V, f = 1 MHz	C_{iss}	–	140	–	pF
Turn ON Time	t_{ON}	–	4	10	ns
Turn OFF Time	t_{OFF}	–	4	10	ns

* Pulse Test Width – 80 μs, Pulse Duty Factor 1%.

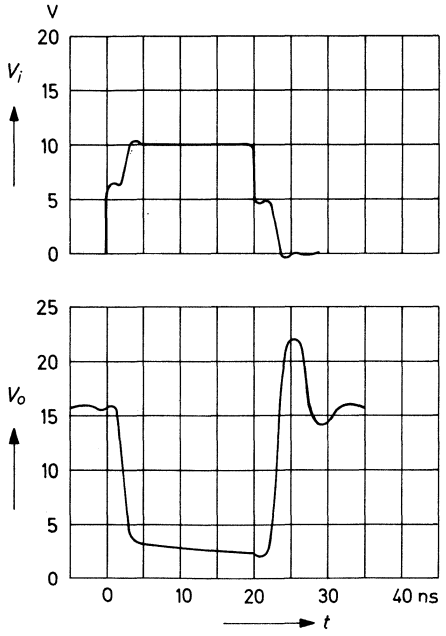


Fig. 6: Switching Performance of Input and Output Voltages (BD 522)

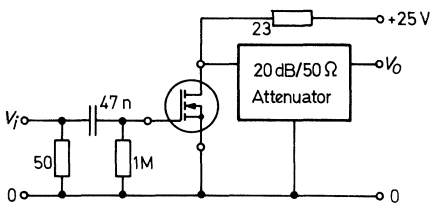
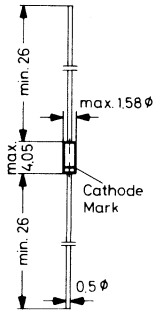


Fig. 7: Test Circuit for the Switching Times (BD 522)

SD101A, SD101B, SD101C

Silicon Schottky Barrier Diodes
for general purpose applications

Special Features:
Low Forward Voltage
Subnanosecond Switching
Glass Hermetic Package



Glass Case JEDEC DO-35

Weight approx. 0.13 g
Dimensions in mm

Description
The SD101 Series is a metal on silicon Schottky barrier device which is protected by a PN junction guard ring. The low forward voltage drop and fast switching make it ideal for protection of MOS devices, steering, biasing and coupling diodes for fast switching and low logic level applications. The SD101A is ITT's equivalent to the 1N6263.

Package Specifications

Lead Material	Iron Core, Copper Clad, Tin Plated
Axial Lead Stress	max. 4.5 N (10 lbs)
Package Inductance	1.8 nH typ.
Package Capacitane	0.25 pF typ.

Absolute Maximum Ratings

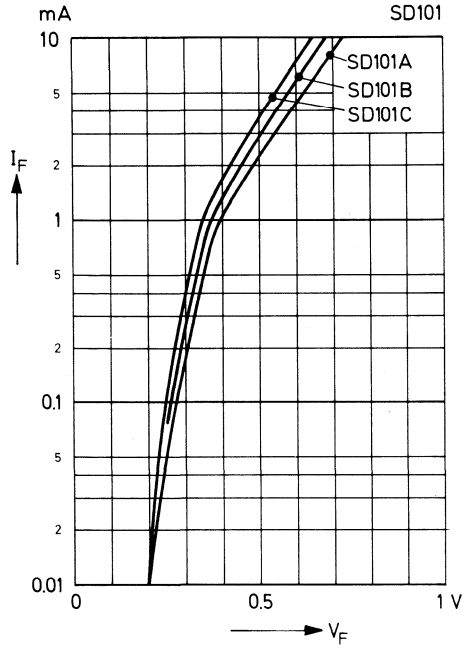
	Symbol	SD101A	SD101B	SD101C	Unit
Peak Inverse Voltage	PIV	60	50	40	V
DC Power Dissipation (Infinite Heat Sink)	P_{tot}	400	400	400	mW
Max. Single Cycle Surge 10 μs Squarewave	I_{FMS}	2	2	2	A
Operating and Storage Temperature	T_j, T_S	200	200	200	°C

Characteristics at T_j = 25 °C

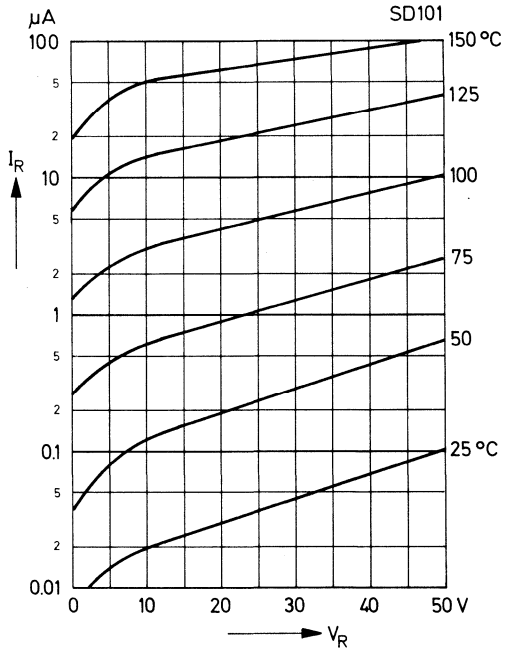
	Symbol	SD101A	SD101B	SD101C	Unit
Min. Reverse Breakdown Voltage at I_R = 10 μA	$V_{(BR)R}$	60	50	40	V
Max. Leakage Current, I_R at V_R	I_R	200 at 50 V	200 at 40 V	200 at 30 V	nA
Max. Forward Voltage Drop at I_F = 1 mA	V_F	0.41	0.40	0.39	V
at I_F = 15 mA	V_F	1.0	0.95	0.90	V
Max. Junction Capacitance at V_R = 0 V, f = 1 MHz	C_T	2.0*	2.1	2.2	pF
Max. Reverse Recovery Time at I_F = I_R = 5 mA, recover to 0.1 I_R	t_{rr}	–	–	1	ns

* JEDEC limit specification on capacitance for 1N6263 is 2.2 pF.

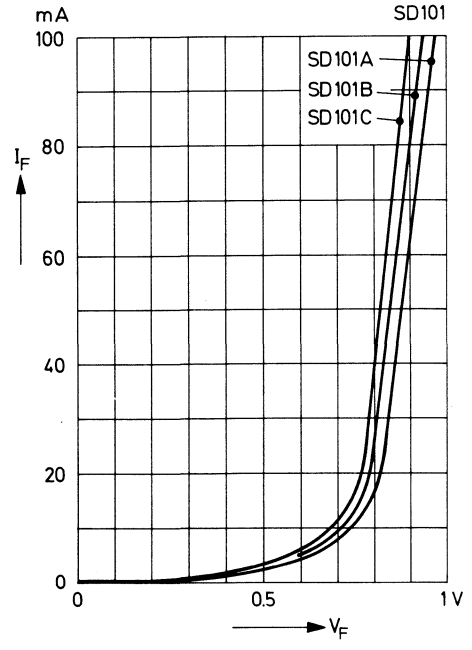
Typical variation of Fwd. current vs. Fwd. voltage for primary conduction through the Schottky barrier



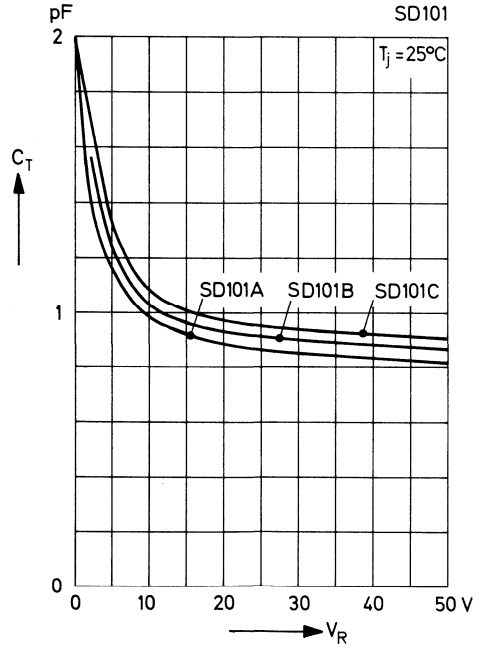
Typical variation of reverse current at various temperatures



Typical forward conduction curve of combination Schottky barrier and PN junction guard ring



Typical capacitance curve as a function of reverse voltage



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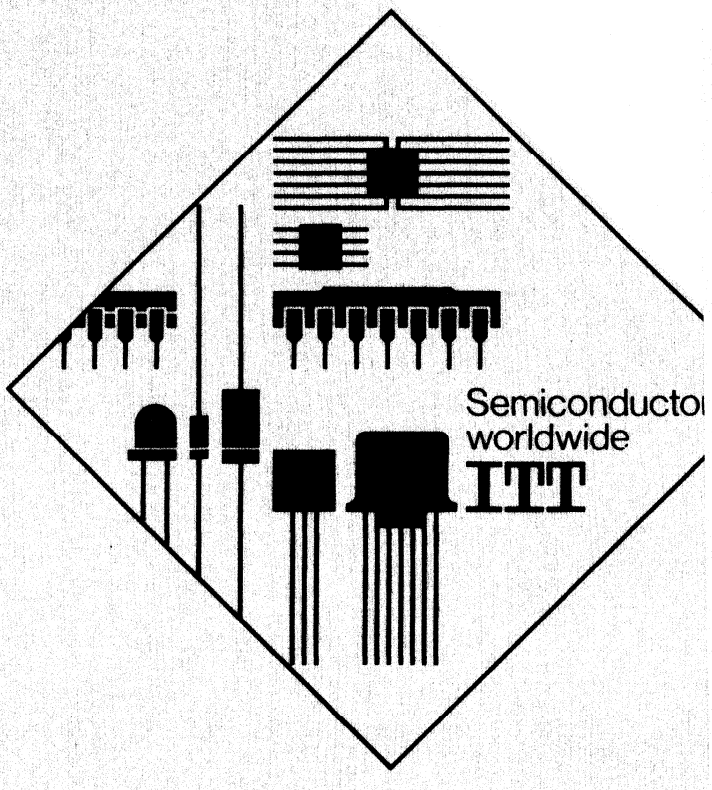

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